INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2001 EDITION

MODELING AND SIMULATION

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MODELING AND SIMULATION

SCOPE

Technology Modeling and Simulation covers the region of the semiconductor modeling world called extended TCAD, and it is one of the few enabling methodologies that can reduce development cycle times and costs. Extended TCAD, within the scope of this document, covers the following topical areas: 1) *Materials modeling*—simulation tools that predict the physical properties of materials and, in some cases, the subsequent electrical properties; 2) *Front end process modeling*—the simulation of the physical effects of manufacturing steps used to build transistors up to metallization; 3) *Device modeling*—hierarchy of physically based models for active devices; 4) *Lithography modeling*—modeling of the lithography equipment and photoresist characteristics and processing; 5) *Equipment/feature scale modeling*—hierarchy of models (except lithography) including the physical environment, conditions, and processes affecting the wafer; 6) interconnect performance modeling—the operational response (mechanical, electro-magnetic, and thermal properties) of back-end architectures; 7) *Circuit element modeling*—compact models for active, passive, and parasitic circuit components, and new circuit elements based on new device structures; 8) *Package modeling*—electrical, mechanical, and thermal modeling; and 9) *Numerical methods*—grid generators, matrix solvers, parallel algorithms, and surface-advancement techniques.

The suppliers of Modeling and Simulation capability include CAD vendors, universities, and laboratories funded by government and/or projects. While a substantial amount of modeling effort takes place inside the semiconductor companies, new modeling capability requires long-range research that is best accomplished in an academic or a laboratory setting. For this reason, a healthy university research effort is a prerequisite for success in the modeling area. It is vital that adequate research funds be made available in a timely manner in order to address the industry's future critical needs.

DIFFICULT CHALLENGES

The difficult challenges in Table 102 are those areas within the scope of Modeling and Simulation that can make the greatest contribution toward solving the difficult challenges of the other technical working groups. It should be noted that a key difficult challenge across all the modeling areas is that of experimental validation. As devices shrink and more materials are introduced into the technology, new analytical techniques that provide the necessary information for this validation of models (i.e., getting the physics and chemistry correct) is critical.

Table 102 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 65 nm, Through 2007	*Summary Of Issues*
High-frequency Circuit Modeling (>5 GHz)	Efficient simulation of full-chip interconnect delay Accurate 3D interconnect model; inductance, transmission line models High frequency circuit models including non-quasi-static, substrate noise and coupling Parameter extraction without RF measurements
Modeling of Ultra Shallow Dopant Distributions, Junctions, and Silicidation	Dopant models and parameters (damage, high- concentration, activation, metastable effects, diffusion, interface and silicide effects) Characterization tools for these ultra shallow geometries and dopant levels
Modeling Deposition and Etch Variations, Feature Variations across a Wafer	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry); reduced models for complex chemistry Linked equipment / feature models CMP (full wafer and chip level, pattern dependent effects) Next generation equipment/wafer models
Modeling of Lithography Technology	Predictive resist models Resolution enhancement techniques; mask synthesis (OPC, PSM) 248 nm versus 193 nm versus 157 nm evaluation and tradeoffs Next-generation lithography system models
Gate Stack Models for Ultra-Thin Dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., MeOx) Model dielectric constant, surface states, reliability, breakdown, and tunneling from process/material conditions

Table 102 Modeling and Simulation Difficult Challenges (continued)

Difficult Challenges < 65 nm, Beyond 2007	*Summary Of Issues*
Complementing Continuum Tools with Atomistic Ones.	A succession of modeling tools that marry atomistic effects with present day continuum software tools
Ultimate CMOS Simulation Capability	Methods and algorithms that will allow prediction of CMOS limits Quantum based simulators
Nano-Scale Device Modeling	New device concepts beyond traditional CMOS based on silicon technology such as vertical MOS, heterostructures, thin-film transistors, single electron transistors
Thermo-Mechanical Modeling for Reliability	Stress voiding, electromigration, piezoelectric effects, fracture, and adhesion simulation tools
Software Module Integration	Seamless integration of simulation modules with focus on interplay and interfacing of the modules in order to enhance design effectiveness

DIFFICULT CHALLENGES ≥ 65 NM, THROUGH 2007

High frequency circuit modeling is a growing challenge as clock speeds continue to increase. Chief among the issues are accurate modeling of interconnect parasitics. Techniques are needed for efficient simulation of full-chip interconnect delay. Accurate models for 2D and 3D interconnect extraction from layout are a continuing need. A sampling of some of the features that must be comprehended to provide adequate model accuracy are the effects of process variations on R, L, and C; partitioning techniques for distributed R-C extractions; and efficient simulation techniques to handle multi-layer dielectrics. The ability to deal with on-chip transmission lines and inductance effects is an increasing requirement. For high frequency modeling, improvements in the transistor models in order to treat non-quasi-static effects, and in understanding the impact of substrate noise are also important challenges. For fast time-to-market, determination of RF models without RF parameter extraction is critical.

The modeling of *ultra-shallow dopant distributions, junctions and silicidation* is a major concern. Thermal budgets have been reduced so much that profiles can be dominated by damage, transient, high-concentration, interface, and surface effects. Obtaining parameters for diffusion and reaction kinetics is a key challenge to allow greater understanding of the processes, especially for new dopants and materials. As low-resistance source/drain extensions are necessary for future high-performance devices, modeling activation/deactivation is key and may lead to achievement of "metastable" dopant activation (higher than equilibrium activation), which may be reduced by transient deactivation due to subsequent thermal cycles (e.g. silicidation, BEOL layer deposition) . More detailed understanding of implant damage, amorphization and subsequent re-crystallization, and silicidation is important, as these phenomena can critically affect dopant profiles. Dopant and defect metrology are critical to the development and calibration of models for profile evolution. Accurate tools do not exist for dimensional (1D, 2D, or 3D) characterization of sub-65 nm technology.

The *modeling of thin film deposition and etch variation and feature variations across a wafer* can provide tremendous savings in development time and cost. For the equipment included in this area—chemical mechanical polish (CMP), plasma deposition and etch, chemical vapor deposition, atomic layer deposition (ALD) and electroplating—simulation is limited by lack of knowledge of the physical properties of materials and the chemical processes needed for these models. The development of accurate reaction paths and reduced chemistry models with only the primary mechanisms necessary for practical applications is an important challenge. Surface chemistry, plasma-surface interactions, and better linking of equipment to feature scale models is needed, both with existing equipment and for next generation (i.e., larger wafer size equipment.)

Modeling of lithography technologies becomes increasingly important in the coming generations as the number of wavelengths and the number of available resolution enhancement techniques increases. Creation of improved modeling approaches for OPC and PSM mask synthesis is an important challenge. Developing predictive resist models is a continuing challenge, but if developed, would greatly expand the application area of lithography modeling. As decisions are nearing on the selection of a next-generation lithography tool (e.g., EUV, EPL, or other alternatives), the development of comprehensive modeling tools are needed to understand the trade-offs between the different approaches.

Gate stack models for ultra-thin dielectrics are needed in order to help optimize very thin conventional dielectrics, as well as to help in the search for alternative dielectric and gate electrode materials. This challenge encompasses the development of a new generation of process modeling tools to help engineer dielectrics on an atomic scale. Furthermore, more detailed quantum modeling of the electrical behavior of the gate stack is necessary as the thickness approaches a few

atomic layers. Fundamental understanding of process impact on the effective dielectric constant, surface states, reliability, and tunneling could play an important role in developing future high-performance MOS devices. There are strong indications that the thin film material parameter values will differ from their bulk values. The material engineering approach based on molecular dynamics simulations and *ab-initio* structure calculations can contribute to the construction of layers with the desired properties.

DIFFICULT CHALLENGES < 65 NM, BEYOND 2007

Complementing continuum tools with atomistic ones—Most of the present day simulation tools use continuum physics. However the need for materials modeling, chemical reactions at the surface, dopant statistical fluctuations, lattice strain effects on diffusion, metastable effects, and quantum effects in devices all point to the need for tools that can bridge from continuum to atomistic models.

The grand challenge for the modeling and simulation effort is to develop software tools to help answer a fundamental question in our industry—what is the *ultimate CMOS technology?* Modeling tools are needed to be able to give guidance through "what-if's," what are the physical limits of the materials, and what are the limits of lithography and device characteristics? When do parasitics, reliability effects, and/or statistical variations dominate? In this regime, non-equilibrium effects will heavily influence carrier transport.

As traditional MOS scaling becomes less effective, *nano-scale device modeling* will be needed to help develop innovative MOS devices as well as to explore new device structures that may operate on different principles. Research on such techniques needs to start very early because a long lead time is anticipated.

The *thermo-mechanical modeling for reliability* of integrated circuit structures has grown in importance. Past efforts have focused on electromigration and stress voiding. Today these areas are just as important, but in addition, thin film and package fracture effects, thin film adhesion and surface roughness predictions, and piezoelectric effects point to the need for increased development of modeling and simulation tools in this area.

There is an increased need for the seamless integration of simulation modules *(software module integration*) with focus on the interplay and interfacing of the modules in order to enhance design effectiveness. Process and device simulators have frameworks that link them. However, little effort has been done on linking other technology modeling and simulation tools. One example would be the linking of the equipment/feature scale simulation tools with a lithography simulator to predict etch profiles for process latitude and sensitivities. Another example would be the linking of chip performance tools with package thermal, mechanical, and electrical simulation tools. A third example is a complete simulation chain linking process modeling, device modeling, compact model extraction, and library generation.

TECHNOLOGY REQUIREMENTS

In the following paragraphs the needs for each of the nine topical areas mentioned in the Scope are discussed in more detail.

MATERIALS MODELING

The determination of the physical properties of thin film and bulk materials and the impact of these properties on the electrical, mechanical, and thermal properties of devices and integrated circuits is becoming more and more important across all aspects of semiconductor technology as new materials are being explored. Both empirical and fundamental materials modeling and simulation are needed to aid in this understanding.

- Many alternate materials are being suggested as possible solutions for some of the critical semiconductor roadmap roadblocks. Materials simulation tools that give insight to inter-relationships between the physical properties of multi-layer thin films and the electrical, thermal, and reliability aspects of the device or integrated circuit would allow "what-ifs" without the need for many and complex experimental characterizations.
- Modeling and simulation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases, these parameters are not known. Databases that contain both experimental and, where not available, material parameters calculated from first principles such as plasma

cross sections, chemical reaction rates, the thermal and mechanical properties of package materials, and interdiffusion constants are needed.

- Materials models are needed for improved resists and for advanced mask making.
- With devices continuing to shrink to nearly atomistic dimensions, materials simulation and modeling tools that go from atomistic descriptions to continuum results will become more and more important.
- For processing, needs include ion implant codes with no adjustable parameters, diffusion kinetics, interdiffusion in thin films, dielectric properties, transport properties

FRONT END PROCESS MODELING

Front end process modeling includes the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding patterning activities. These areas are important for understanding and optimizing transistor fabrication. The needs for modeling are driven by the reduction of feature size in scaling transistors, which not only cause higher demands on model accuracy but also requires models for currently not considered materials, material properties, or dopant species.

As technology scales, the requirements on implant energies are pushed to sub-keV energies, requiring understanding of the surface interactions (including reflection and sputtering) and the nuclear stopping power. For wells, energies are being pushed to the MeV range requiring better understanding of electronic stopping mechanisms. Key to both efforts is damage reduction. The damage interacts with both dopant diffusion and activation, and creates transient enhanced diffusion (TED), which can produce junction shifts on the order of several hundred nanometers. Reduction of thermal budgets to minimize diffusion and junction shifts is in competition with the need for sufficient dopant activation. Significant effort needs to be expended to understand TED and activation well enough so that the necessary trade-offs between both effects can be optimized. Despite more than a decade of work in this area, sufficient quantitative predictive models are still not available. Models need to also consider experimental conditions different from the traditional furnace anneals, especially Rapid Thermal Annealing and Laser Annealing.

Analytic models will continue to be needed for ion implantation simulations in the near term. Model data sets need to be extended to include damage, In and Sb in silicon and silicon-related materials, as well as very low (about 1 KeV) and high energy (some MeV) implantation. Channeling tails need to be modeled for the full range of tilt and rotation conditions and relevant layout stacks. As the lateral profiles become more and more important and complicated, accurate lateral doping and damage distributions need to be modeled. Monte Carlo implant models will be needed to support analytic model development, and for application in cases that cannot be adequately addressed by analytic models, e.g., doping of sidewalls of narrow trenches. To accurately model dopant and damage interactions from source/drain and pre-amorphization implants, models for amorphization layer depth, dislocation loop evolution, and residual TED need to be developed. Extensive research and model development needs to be started immediately to develop improved models for damage creation and annealing, and for temperature-dependent implantation. Predictive models need to be developed for advanced doping techniques, like solid source, plasma implantation, GILD, and vapor phase doping. As no technique has emerged as a clear winner so far, the modeling community needs to monitor the evolution of these techniques and develop models for the most promising ones.

For dopant diffusion and activation, continuum models will remain the mainstay of process simulators, and will need refinement due to smaller devices requiring higher accuracy and new effects emerging. Point-defect based diffusion models will need to be considerably refined especially concerning the interaction of dopants and defects in clustering and activation, and dopant binding. RTA ramp rates are an important factor, and their influence in diffusion/activation models needs to be tested. The effect of interfaces, especially non-SiO_2 interfaces, will become increasingly important. Here, the segregation and trapping of impurities needs to be modeled for all kinds of gate dielectrics, including SiO_2, nitrided oxides, and high κ materials, and taking the influence of N, C and F impurities and of knock-on oxygen into account. To complement experimental work, atomistic process models will be used to contribute coefficients for continuum models. For example, dopant binding and migration energies need to be calculated, such as the binding energy of a substitutional dopant to a mobile interstitial, the migration energy of the dopant-interstitial pair, and the binding energy between a mobile dopant atom or silicon interstitial and a point defect or dopant cluster. Forward and reverse rate coefficient calculations will be needed for several types of dopant-defect and dopant-interface interactions.

Advanced process models will be needed for the modeling of metastable dopant activation (>solid solubility). These should include the deactivation kinetics during subsequent backend processing.

Models for surface and interface diffusion will be needed. These include interactions with SiO_2 and new gate dielectric materials. Process models for alternative materials (such as SiGe or SiGe:C) also need to be developed.

With rapidly shrinking device dimensions, mechanical stress effects are becoming important, and models for the effect of stress on reliability and dopant diffusion need to be developed. Stress resulting from all process steps must be considered over the full range of temperatures used in processing. Thin film growth needs to be better understood, including the reliability impact of stress in corners and small 3D structures. Characterization of films with small dimensions and thickness is critically important but extremely difficult. In fact, all models need extensive characterization, which has been difficult and expensive.

There will be a continuing need for silicidation models in the near term. Gate dielectric process models, including models for non SiO_2 dielectrics, will be needed to accurately predict gate stack properties and dopant profiles in the channel and source/drain regions. For gate stack modeling, kinetics of oxidation with N_2O, NO, and N are needed. Species influencing oxidation kinetics may be intentionally introduced in additional process steps, like implantation of nitrogen, or be part of the process gas, or result from contamination. All these effects need to be modeled. Visco-elastic oxidation models need to be calibrated for whole ranges of process conditions, nitrided oxides, and orientations as required for advanced isolation architectures. In the near term, activation models for polysilicon gates will be needed. In the long term properties of gate electrodes will need to be modeled.

Deposition and etching models on feature scale need a link to equipment simulation with respect to the coupling to the process parameters set by the operator at the equipment and to predict the homogeneities of results on the wafer and between different wafers. This should also result in more physical feature scale models.

In the long-term years of the Roadmap, atomistic process models will be required for direct simulation of front-end processes, in addition to the application to model development and parameter extraction mentioned above. Procedures for utilizing *ab-initio* calculations into the mainstream TCAD models need to be developed.

Improved metrology and analytical techniques are very essential for the determination of accurate process models.

DEVICE MODELING

Device modeling includes a suite of approximate models and methods to describe charge carrier transport, the electromagnetic field and in some cases also energy transport. Models cover drift-diffusion, hydrodynamic, energy transport and Boltzmann equations. Methods include deterministic numerical methods like finite differences, box integration and finite element and stochastic ones like the Monte Carlo method. Various combinations of models and methods result in differing accuracy of the description and computational burden. This model suite has to be extended to include approximate quantum modeling. In some aspects, such as non-local effects due to impact ionization, band-to-band tunneling, trap-assisted tunneling or channel mobility, the basic physical models have to be refined. Moreover, CAD tools should indicate the conditions when changing models is recommended, either because otherwise important physical effects will be ignored in the result or the computational effort is unnecessarily high. Means have to be provided to facilitate shifting between adjacent models in a consistent fashion.

Within the scope of advanced BiCMOS device development the base engineering has led to new architectures exploiting SiGe and SiGeC base technology in order to minimize boron diffusion out of the base. Support of RF, analog and mixed-signal BiCMOS circuit design requires enhancements of respective support in numerical device simulation. Efficient post-processing tools are needed to analyze device performance, to characterize non-quasi-static effects, to minimize the requirement for time- and cost intensive RF measurements and to provide predictive data in the downscaled regime. Device simulation integrated with RF circuit simulators or mixed-mode simulation will ease optimization but requires very efficient algorithms to be useful. Approximate models for surface-quantization and direct gate tunneling have to be developed. Comprehensive internal noise modeling must cover each important internal noise source from the sub-kHz to the at least 20-GHz regime. Efficient models for substrate noise coupling have to be provided to couple comprehensive descriptions of external noise sources to the transport equations in a flexible way. Self-heating of chips must be taken into account. With shrinking device dimensions, the contact resistance will become a larger and larger percentage of the total device resistance (channel, S/D, contact) and as such will play a more important role in predictive simulation of the current-voltage characteristics and transconductance.

Simulation for large area devices also needs to be explored. Power amplifiers or optical devices are usually built from many transistor cells connected together through a huge interconnect system. The impact of distribution effects on device

parameters is not well understood and modeled, where thermal and electromagnetic effects are key. Large signal behavior is required in most cases. A complete simulation by the means of the traditional TCAD approach is not possible, since the number of grid points would be too large.

Transport phenomena have so far focused on bulk silicon. For 100 nm devices and below, the gate dielectrics are so thin that tunneling gate current will become a very important design factor. More detailed quantum modeling of the entire gate stack (channel, dielectric, electrode) is needed in order to understand oxides and nitrided oxides that are only a few atomic layers thick. Finally fundamental material modeling should be intensified to aid in the search for and evaluation of alternative gate dielectric materials to understand the impact of new gate dielectric materials. Such modeling should include details of tunneling and transport in the dielectric, reliability effects, interface states (at all intermediate interfaces), impact on channel mobility and detailed understanding of effective dielectric constants of a complex dielectric stack. Models for non-volatile memories still need significant improvements.

As classical MOS devices continue to scale, it is important to understand possible limits to scaling from a modeling perspective. For example, the effects of statistical dopant fluctuation or of variations in gate stack line width need to be simulated. Realistic pictures of the dopant profiles prevent a decoupling of the various directions in the device such that often a full three-dimensional problem must be solved.

With the pursuit of ultimate CMOS, a large variety of new device architectures are proposed.[1] A very promising method to suppress the short-channel effect exploits thin-film SOI. Other new device features include non-planar or elevated S/D structures, strained heterostructures in the channel, vertical FETs and other structures with double-gate or a surround-gate. Memory technologies have to investigate para- and ferroelectric as well as magnetic structures.

For ultimate CMOS as well as for novel device architectures more rigorous models are required. The short distance between source and drain (down to 22 nm) and film thickness below 10 nm require a full two-dimensional quantum transport formulation of the I_{on}, I_{off} and I_{gate} currents. Several approaches have been suggested to realize these calculations, but they all suffer from rigorous justifications where to truncate the approximation. The simplest scheme is based on a self-consistent Poisson-Schrödinger coupled set of equations, whereas more advanced methods attempt to use Green's functions or to solve the quantum Liouville equation either formulated in Wigner functions or in moments of these functions leading to a quantum drift-diffusion model. Apart from the formal justification of the computational algorithm the CPU demand also is huge. Memories require the modeling of spin and magnetic interaction.

To address design for manufacturability (DFM) issues and methodologies a representation and common language of device variability (doping, gate line width etc.) has to be developed and interfaced to circuit design.

Rather good progress was made in the last decade for the modeling of substrate current and hot carrier injection effects. Applications of microscopic simulators have created a detailed understanding about the generation and dynamics of hot carriers. However, super scaled devices, especially with then dielectric layers, require further development in this area. Degradation models are first priority. Developments on bipolar technologies are still behind models for MOS devices. Prediction of AC reliability is also an important question.

This roadmap addresses mainstream silicon needs. Compound semiconductor technology needs are being identified, and it is anticipated that future roadmaps will address needs in this area. *A link to an overview of this topic on compound semiconductors is provided.* Lithography Modeling

Lithography modeling and simulation needs have been sub-divided into four areas; resist modeling, overlay, defect simulation, and lithography technology and techniques. These areas are discussed below and summarized in a Lithography Modeling and Simulation Needs and Potential Solutions table given in the *Lithography* chapter of this Roadmap.

- *Resist modeling*—Predictive, quantitative resist modeling will continue to be the bottleneck in predictive lithography simulation. Models for chemically amplified resists that include post exposure bake, diffusion, line edge roughness, and surface interactions are needed. Thin and multilayer resist models that link the lithography to the etch process are becoming important. And there is a growing need for resist studies based on computational molecular modeling.

[1] *Mark Lundstrom, Supriyo Data, Philip Bagwel, "Modeling and Simulation Issues for Revolutionary Electronic Devices", Electrical and Computer Engineering, Purdue University, August 13, 2001.*

- *Overlay*—Overlay continues to be a major lithography issue. Improved models for alignment signals, for feature size dependent pattern placement, and the potential next generation lithography tools are required.
- *Defect simulation*—Techniques for modeling defect printability from mask through final product are needed.
- *Lithography technologies and techniques*—Lithography technologies modeling needs include not only improvements for standard optical systems but also for next generation lithography techniques.

An important application for the next few technology nodes will be evaluation of the trade-offs for the various lithography options (such as 248 nm versus 193 nm versus 157 nm on specific critical layers). In order to fill this requirement, better imaging models, which include the non-idealities of the respective imaging systems, are needed. Lithography at its limits requires a better modeling of image formation for very high NAs, associated aberrations and polarization effects. Furthermore, improved resist modeling and characterization capabilities at the given wavelengths need to be developed and coupled to the imaging models.

For next-generation lithography technologies, there is a need to have reliable simulation tools for extreme ultra violet (EUV), for direct e-beam, for electron projection lithography (EPL), and for maskless lithography (ML^2) techniques.

Lithography modeling techniques include phase shift, high numerical aperture, surface roughness, and scattering effects. Electromagnetic scattering analysis will need to become part of the mainstream investigation capability. Scattering from phase shift masks, and scattering from wafer topography underlying the resist are two examples of applications requiring rigorous electromagnetic capability.

Finally, integrated modeling systems are needed to analyze and optimize future lithography processes. With so many independent parameters, and an avalanche of data to understand, computer-based optimization systems are a requirement to fine tune future technologies that will operate near the limit of diffraction optics.

EQUIPMENT/FEATURE SCALE MODELING

The key driver for accurate equipment/feature scale modeling and simulation software tools is the need to obtain knowledge and insight that will reduce development cycle times and costs. Enablers for equipment modeling are materials and process simulation tools, equipment to feature scale simulation capabilities (including equipment-feature integration), process control, and sensor design.

The equipment/feature scale modeling area can be subdivided into several unit process areas: CMP, plating, thermal and RTP, and plasma processing (CVD, PVD, etch). The requirements vary per application and per process being considered (such as thermal, deposition, etch). Thus, the metrics in Table 103b express accuracy requirements as a percent of specification limits or metrology capabilities. Models ranging from easy-to-use to complex, from fast executing to computationally intensive, and from high accuracy in a constrained process space to moderately predictive over wide range should be available to satisfy all uses. As the application moves from equipment understanding toward process integration, the need for linkage between equipment models and wafer/feature scale and atomistic models becomes stronger.

Although the models are becoming increasingly predictive, validation is still critical before results obtained from simulations will be considered. As a bare minimum, equipment and feature scale models must be able to predict trends correctly (correct sign and order of magnitude) to be useful. These two simulation areas (equipment and feature scale) must also become tighter linked so that process variations across a wafer and from wafer to wafer can be studied.

Fundamental physical data such as reaction mechanisms and rate constants (both gas/plasma and surface) are key to properly capturing the physics and chemistry of surface evolution during thin film etching or deposition. Both experimental and computational methods are needed to obtain these mechanisms and rate constants. A hierarchy of computational approaches from atomistic (molecular dynamics, Monte Carlo, quantum chemistry) to continuum must be employed (see the *Materials* section in this chapter for more discussion). Providing integrated equipment and feature-scale simulation remains a great challenge as the fluxes from the reactor determine the boundary conditions for the feature scale and vice versa. Understanding derived from both the equipment and feature scale areas is also needed for modeling pattern dependent variation.

An important future application of equipment modeling is the control of manufacturing equipment based on real time simulators including sensor design and simulation. Sensor design includes determination of what to measure, where to

locate the sensor, as well as creation of "soft sensors," such as the use of a model to predict a quantity of interest from available measurements.

The potential solutions for equipment/feature scale modeling have been divided into six categories:

1. *Rates*—The understanding of semiconductor processes is improving, and the advance of computer capability is allowing one to solve large and difficult problems more effectively. However, chemical kinetics of bulk and surface reactions needs attention. These input parameters to the simulation codes are many times the weak link in being able to accurately predict results. Experimental determination or quantum chemistry methodologies for calculating these needed parameters would provide potential solutions.

   In addition, many times the complex chemistries can be reduced to a reduced model requiring only a few equations, thus allowing faster results and better insight into the driving mechanisms.
2. *Reactor modeling*—Plasma modeling and simulation is one of the more difficult unit process simulation areas. Accurate plasma models, the link of these gas phase models to the features on a wafer (such as good sheath models), and the ability to predict the equipment related variations across a wafer would lead to a significant improvement in process understanding.
3. *Feature scale models*—Present feature scale models are continuum models. They do not take into account grains, grain orientations, stoichiometry, composition, and interfaces. However, these materials considerations dictate the electronic and mechanical properties of the thin film layers. Predictive simulation solutions to these problems are only now becoming feasible.
4. *Chemical-Mechanical-Planarization models*—CMP is a difficult chemical-mechanical problem. First order models and simulation tools exist. However, with CMP being used on a variety of dielectric and metallic materials, better predictive models are required. For example, models for feature-scale CMP modeling are needed to analyze dishing/erosion effects in the copper Damascene process. Of high priority is the quantitative understanding of the planarization of porous low κ materials. The impact of tiling (placing dummy features on the wafer for arriving at the desired end result after CMP) needs to be understood on a CAD level as is done for mask designs in lithography.
5. *Interconnect morphology and reliability*—Materials models and simulation capability in this area would accelerate the development of new technology nodes since now over half of the total process is related to that above silicon.
6. *3D discretization*—3D discretizations are very important and only partly resolved. In equipment simulation this refers to the user-friendly and CPU efficient discretization of process chambers including the wafers to be processed, whereas in feature scale simulation the specific problem is the accurate and reliable discretization of time-dependent geometries. Combined equipment/feature scale simulation is faced with all these problems and also the problem of the different length scales involved.

INTERCONNECT PERFORMANCE MODELING

Interconnects are of key importance to circuit and system performance. Downscaling implies that operation conditions are pushed to limits where, without precautions, failure mechanisms will be ubiquitous. Electromigration, stress voiding, and extrusion are a few examples. Besides the physical damage mechanisms, other failures exist related to signal integrity. The specific precautions refer to process conditions, the use of alternative materials and stacks as well as designs. Therefore, just as in the front-end technology, two areas may be identified—the modeling of the processing (the *Equipment/Feature Scale* section) and the modeling of the performance of the back-end architectures based on the process, which this section addresses.

Of high priority are the coupled thermal and mechanical performance properties of thin multi-layer films. Structural and compositional properties of thin films need to be obtained and related to reliability effects. The mechanical properties of these thin films, such as fatigue, fracture, and stress voiding, also affect reliability performance. Thermal cycling can trigger fractures that may not be foreseen. Simulation tools are needed to more effectively study these effects than by experiment alone. The interplay with equipment and feature scale simulation becomes an increasingly important factor for being successful. The change to low κ dielectrics with low thermal conductivity have placed much more emphasis on combined electrical and thermal modeling in the suite of modeling and simulation tools needed for interconnect technology development.

As the operation speed of devices is increasing to the multiple GHz range and the complexity of interconnect systems continuously increases, software tools with higher accuracy and better efficiency become necessary. Accurate modeling of high frequency electromagnetic properties like inductive coupling is key.

The ability to predict the electrical and parasitic properties of complex interconnect structures continues to be a challenge. Software tools and methodologies that link process results to results at the IC level, that identify reliability issues or design deficiencies, that give the designer capabilities to explore alternative interconnects easily are needed.

CIRCUIT ELEMENT MODELING

A solution to the present design productivity crisis requires modeling improvements that encompass many of the implementation issues faced by a design team. Historically the modeler's role has stopped at an accurate physical model of the transistor and the interconnect system. However, the large increase in chip size and complexity, coupled with the re-use of many circuit structures, partitions, boxes and even entire chips requires sufficiently accurate models of all these structures.

Compact modeling (for both transistors and interconnect) and circuit simulation are the first key to chip design productivity. The challenges are the drastic increase of clock frequency, the decrease of "headroom" (voltage between V_t and V_{dd}), increased time spent in the subthreshold and weak inversion regions, and the exponential increase of the circuit complexity. Two opposing requirements always need to be met—accuracy and CPU efficiency. This dichotomy gives rise to a hierarchy of models. The most accurate models will be used only for simulation of small circuits. Less accurate models will be derived from these for simulation of larger circuits, and so forth. Historically analog simulation needs have driven the development of circuit simulation models, which are then used by both analog and digital design teams.

For today's competitive analog designs accurate DC and high-frequency AC models for transistors, interconnect, passive, and parasitic elements are required. Bipolar transistors are very important for those applications. Model improvements for sub-100 nm need to address velocity overshoot, quantum effects, source barrier effects, noise behavior, and non-quasi-static behavior. Low-voltage technologies emphasize sub-threshold and conductance behavior.

Interconnect delay forms an increasing fraction of critical path delay in current and future technologies. Improving the accuracy of extraction of interconnect parasitics from layout and ideally process databases is an important requirement; accommodating complex geometries (such as 3D effects) and accurately modeling cross-talk are key issues. At higher clock frequencies, complex electrical effects will be significant, such as inductive coupling, ground bounce, transmission-line, and skin effects. Mismatch in interconnect is a limiting factor for very high speed processors.

As was noted in the *1999 ITRS Design* chapter, correct-by-construction design is a requirement because verification is costly (both in time and resources). Even if an original flagship design could afford the verification time, scaled and derivative designs are always under extreme time pressure. Structure modeling and sensitivity analysis is needed to avoid many costly implementation re-simulations in areas such as noise margin, writeability (determination of voltage necessary to change the state of storage cells), keeper sizing, etc. For instance, in the case of writeability, much of the work of performing simulations to check writeability of circuit structures can be automated. However, fixing all the problems that were uncovered will take time. If a sensitivity analysis could be done in the first place, the original design could be completed with sufficient margin such that a minimum number of changes will be required during scaling.

Similarly, reliability checks for effects such as electromigration and hot carrier effects could also be modeled and analyzed such that a full re-verification is not required for every new technology. It is not uncommon for such reliability verification tasks to consume as much time as many of the implementation analyses. Models that treat such reliability concerns (as well as ESD, SER, and oxide reliability), will become increasingly important for circuit design. Analog, RF and system-on-a-chip applications will create new demands, for example noise concerns in RF circuits.

With the trend toward providing multiple transistor options (high-V_t, low-V_t, thick oxide, etc) for every technology, each must be characterized for all relevant device structures, such that the benefits and risks of device substitution within structures during scaled chip implementations are easily understood. A significant amount of statistical analysis is implied in these concepts. The modeling must encompass variations of the present technology as well as variations in future ones.

With the strong need for RF circuit design tools, it will be important to incorporate more materials properties and physics in the design environment. Both active and interconnect models need to be characterized for process variations. For example, the variation in interlevel dielectric (ILD) thickness using CMP is more than 20%. Robust parameter extraction for these complex models will be a significant challenge. The development of industry-standard circuit models is also necessary to support the current business environment, in which design and manufacture often take place in different companies.

In the future, when the device switch is no longer the familiar MOSFET, models must be developed to predict and analyze the impact of the new devices on the inherited structures from a previous generation. There must be more emphasis on

new circuit techniques that can form a tight link between the physical properties of the 'switch' and the desired circuit function.

Since the length of the transition period from "switch=MOSFET" to "switch=x" is unknown, modelers must be prepared to cope with demands for models for many novel device types. Further, it is certainly conceivable that we will never again have the luxury of technologies that only require two device types: n-channel MOSFET and p-channel MOSFET. More likely, the modeler must comprehend interactions between several different device types, including electrical, optical, and mechanical devices. Signal integrity is already a large concern. In the more complex post-MOSFET environment it will be overwhelming without careful modeling performed in a hierarchical manner with careful accounting of interface interactions.

PACKAGE SIMULATION

Packaging needs to meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries. A key challenge is the need for co-design of electrical, thermal, and mechanical aspects, both on- and off-chip. These phenomena can no longer be described independently. The use of co-design tools will also drive the need for parameter "passing", for improved numerical methods to handle the complex structures, and methodologies for being able to explore tradeoffs of accuracy versus time to obtain the results.

Improved reliability models for package design and development are needed. Built-in and thermally induced mechanical stresses need to be modeled throughout the 3D stack, coupling the chip and package level. The introduction of low κ dielectrics with low thermal conductivity amplifies the need for accurate thermal simulation, which needs to be solved consistently with electrical behavior given the higher power dissipation levels. Strongly non-uniform heat dissipation across the chip further complicates this analysis and emphasizes the need for die-package coupling. Predictive software tools for fracture, stress migration and voiding, and fatigue in thin films are needed to understand the coupling between the package mechanical properties and the chip.

Power delivery for high frequency devices has become a major issue. Modeling inductance loops and analyzing return paths that extend over both the package and chip pose a complex problem, for which more powerful, integrated simulation systems are needed. Ideally, simulation systems should generate results working directly from the package and chip layout databases, creating accurate 3D representations of all interconnects.

The modeling of electrical signal propagation needs to be improved substantially from approximate RLC modeling to full transmission line modeling. Circuit simulation tools need to couple board to package to chip. Electrical modeling must expand to include digital, analog, and RF devices on the same package or die. Noise coupling through power distribution networks and electromagnetic interference are areas of special concern for system-on-a-chip or system-on-package approaches.

NUMERICAL METHODS AND ALGORITHMS

Numerical methods and algorithms need improvement to support the growing complexity of physical phenomena to be addressed by extended TCAD. For example, more accurate solutions of the Boltzmann transport equation in device simulation, or the inclusion of stress and of several defect species and complexes in the simulation of dopant diffusion and activation requires dealing with an increasing number of coupled partial differential equations over the device grid. Moreover, physical processes with different intrinsic time- and/or length scales critically influence each other, and have to be simulated adequately in a coupled manner—point-defect diffusion occurs on an orders of magnitude faster time scale than macroscopic process time. The gas flow, depletion, and reaction in an oxidation furnace on a macroscopic scale are the basis for the chemical vapor deposition in a contact hole, there also critically affected by the local geometry on a deep sub-micrometer scale. These are just some examples how increased requirements on predictivity and accuracy of models cause more complex models and, in turn, drives discretization methods and linear solver technology, especially for the solution of large systems of coupled diffusion-reaction equations and/or transport equations.

Increasing accuracy requirements lead in many domains of modeling to the transition to a completely different level of approach, such as Monte-Carlo instead of analytical simulation of ion implantation, atomistic simulations instead of continuum diffusion equations, rigorous solutions of Maxwell equations instead of the traditional thin mask approximation to enable the simulation of advanced masks (phase shifting masks, optical proximity correction) in optical lithography. These more complex modeling approaches frequently require the development of new problem-specific and efficient algorithms, as the application of standard algorithms would result in prohibitive time and memory requirements. In consequence, the state-of-the-art of the numerical methods and algorithms available or being developed mainly in other

domains of science must be permanently checked from the point of view of the application requirements of all domains of simulation, described in this roadmap, and be used to influence and kick-off developments required.

Meshing, although always important for the efficient and accurate solution of differential equations, has become a key problem due to two-dimensional simulations being more and more complemented by three-dimensional simulations of critical devices, structures, process steps, materials, or fabrication equipment. Moreover, the increase of the numbers of steps to be included in process simulation, and especially the frequent use of automated simulation splits to investigate process options and the sensitivity of electrical device data on process details, requires completely automated grid generation. This automated grid generation must be reliable for all kinds of device geometries and distributions of volume variables, with a failure rate at least two orders of magnitude below current tools. In addition, meshing tools must be capable of resolving all critical features of the device, like small geometry features or steep dopant gradients, without unacceptable drawbacks in terms of mesh nodes or computation time needed for mesh generation or adaptation.

Mesh generation time is especially critical in case of simulation splits or simulation runs with a large number of process steps. Considerable problems are caused especially in three-dimensional simulations by moving gradients of volume variables and even more by moving geometries: These require parallel mesh refinement and unrefinement or the use of moving mesh nodes, in most cases with additional requirements on the shape or quality of the mesh elements to be met to enable an appropriate solution of the physical model equations to be solved.

Meshing algorithms must make sure that discretization errors caused by the removal or by the movement of mesh nodes do not negatively affect the simulation results: Especially for applications in sensitivity analysis it must be guaranteed that changes of the results are due to physical reasons and not critically affected by changes of the meshes used in the different simulations.

A favorite solution to this problem is that a new mesh should use as many nodes and elements of the preceding mesh as possible and appropriate, such as during the simulation of oxidation. Stable and efficient algorithms are needed to trace the change of device geometries especially in the three-dimensional simulation of process steps like etching where multiple layers have to be considered. Such algorithms must reliably avoid artifacts in device topology and allow for appropriate volume meshing. Currently, none of the several approaches used (triangulated surfaces, cells, level set; delooping) has demonstrated to solve all relevant application problems.

These meshing requirements outlined above are further extended by the growing demand for equipment and material simulation. While in this case the problem of moving geometries hardly exists, adaptation to time-dependent volume variables is still critical. Automatic mesh generation and adaptation is especially important to resolve critical features of equipment geometry and the wafers to be processed, while avoiding a too high number of mesh nodes. This problem gets even more severe when coupling equipment and feature scale simulation. Several current tools for Computational Fluid Dynamics (CFD) calculations suffer from a complicated procedure to define the geometry to be simulated and to provide necessary information for mesh generation. Although the mesh quality criteria in these applications differs considerably from. process and device simulation, also.in equipment and materials simulation a key problem is finding ways to efficiently generate appropriate discretizations of the geometries to be described and automatically extracting the necessary information to control the volume meshing tools in terms of local mesh spacings, mesh orientations, and quality criteria.

Particle-based Monte-Carlo codes need an increase in raw CPU speed as well as variance reduction techniques to minimize noise within acceptable simulation times. The rapidly increasing demand for more MFLOPS will at least be partly met by improving hardware, provided current trends continue. Workstation speed has improved by 1.8× on average each year since 1990. Parallel solution strategies are also needed in order to address computationally intensive 3D simulation needs. This especially includes the use of distributed systems (e.g., workstation clusters), where data exchange between the processors must be minimized by the algorithm. These systems are currently standard in industry. However, it has to be critically investigated which kind of simulations will only be possible with large shared-memory computers, and whether and how sufficiently powerful systems will be accessible to industry and research.

DISCUSSION

In some cases the Modeling and Simulation software tools have begun to be linked together (such as traditional TCAD process and device simulators, design tools), while in many other areas the software tools are still separated. If one examines the cycle time for development of a new technology, much of that time and cost is not in the individual module development, but at the integration level. There is a continued strong need for Modeling and Simulation tools to be better linked for determining unforeseen interactions of one step on the next. This type of effort is needed for the following:

1. The interfacing of materials structural simulation tools with software that predicts electronic properties. An example where these tools would be useful would be in the development of high κ dielectric thin films. Future software tools in this area then might treat the gate stack as a system rather than as individual components. Unforeseen materials interaction issues, better "what-if" analyses, and reliability effects could be studied.
2. The interfacing or integration of individual equipment/feature scale simulation tools. An example would be the linking of a lithography simulation tool that predicts exposure characteristics in photoresist with a plasma etching tool that predicts etch profiles for process latitude and sensitivities.
3. Structured data sets that contain needed physical constants that facilitate parameter passing between tools.
4. The integration of chip performance tools with package thermal, mechanical, and electrical simulation tools to create a co-design environment.
5. The integration device simulators with robust methods for creating compact models and device files for design.

CAPABILITIES AND ACCURACY/SPEED REQUIREMENTS

Modeling and simulation encompasses a variety of applications with widely varying requirements. For example, in applications closely associated with design, speed and accuracy of phenomenological models are the primary requirement, while predictability in uncalibrated regimes is secondary. Examples are circuit modeling and the lithography models built into OPC systems. In applications associated with technology development, the requirement may be considered to be a mixture of physically based models and characterized empirical models. Traditional TCAD applications, when used to optimize technology development (using highly characterized simulators), fit this description. Finally, there are modeling areas in which the basic physics are being explored. Examples are Monte Carlo device simulators, or first principles calculations of diffusion parameters for dopant diffusion in silicon. To give useful guidance for all these application areas, the Technology Requirements tables for Modeling and Simulation have been divided into tables for simulation "Capabilities" and tables for "Accuracy and Speed." Refer to Table 103a, b, and c.

The "Capabilities" requirements tables (Table 103a and c) are meant to describe the technology requirements for Modeling and Simulation that demand new areas of modeling be developed. An example would be the capability to model EUV lithography steppers. In this case, the basic ability to simulate the performance of an EUV stepper needs to be developed. This type of requirement is often tied either to the introduction of new technologies or to new regimes of physical phenomena at smaller dimension.

In contrast, the "Accuracy and Speed" requirements table (Table 103b) more properly describes the level of simulator accuracy needed for process/circuit design or optimization. For TCAD applications, this level of accuracy is needed to achieve the overall TCAD cost reduction goals listed in the first row of the table. The cost reduction goal should be interpreted more generally as a cost and development time reduction, as it is understood that TCAD should speed up the process development schedule. For ECAD and design applications, these are the accuracy levels needed for designers to effectively create new products. Note that accuracy requirements are specified only for the short-term technology requirements; for the long term, investigation of new technologies is the overall priority. It should be recognized that at a given point in time, several technology generations are being simulated in parallel, with differing accuracy requirements for each.

It should be noted that the accuracy requirements in Table 103b refer to accuracies obtained after calibration of the simulation tools to a particular technology node. It is generally understood that for TCAD simulation tools in particular, calibration is required for each technology node because new technologies, materials, dopant species, and process regimes are introduced in each node. The accuracy numbers were determined by questioning a sample of process development and design engineers.

Table 103a Modeling and Simulation Technology Requirements: Capabilities—Near-term

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ PITCH (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
Lithography							
Lithography: evaluate wavelength	**Evaluate 248 nm versus 193 nm**		**Evaluate 193 nm Versus VUV**		**Evaluate VUV versus EUV,EB**		
Resist models	**193nm resist models**	**157 nm resist models**	**Detailed chemical resist model**				
Front End Process Modeling							
Gate Stack: evaluate materials	**Model alternate dielectrics and gates (interfaces, impurity diffusion, barrier height)**				**Materials to electrical properties**		
Diffusion and activation models	**Interfaces, stress, ultra-shallow junctions, Si:Ge:C, source/drain.**			**Move from calibrated phenomenological to physically based models**			
Back End Process/Equipment/Topography Modeling							
Models for multi-level metal	**Mechanical/thermal stress and cycling**		**Stress voiding, adhesion, and fracture**				
Planarization models	**CMP/dummy features**		**Full CMP model**				
Equipment/feature scale link	**Plasma deposition and etch models**		**Litho/plasma integrated model to predict within-chip feature variation**				
Device modeling (Numerical)							
Bulk CMOS	**Gate current models; gate oxide reliability**		**Full quantum gate stack models; device models with relevant quantum effects included**				
Non-bulk CMOS	**Heterostructures; stress dependent mobility model for Si:Ge:C**		**"What if" capability for non-bulk CMOS devices**				
RF Modeling	**Noise models**		**Frequency, noise, parasitic device tradeoffs**				
Circuit Element Modeling/ECAD							
New circuit element models	**SOI circuit model**		**Non- bulk CMOS compact models**			**2D quantum effects / non-quasi-static models**	
Interconnect models	**Full-chip RC**		**On-chip inductance effects, full chip RLC**				
Design/device links	**Ioff/Ion link**		**Best practice analysis for design**				
Package Modeling							
Package models	**Complex interconnect geometries**		**Thermo-mechanical-electrical integrated models**				
Unified package/chip models	**Co-design package / circuit models (multiple power and ground planes)**		**Unified RLC extraction for package/chip**			**Full-wave analysis**	
Numerics							
Numerical algorithms	**Robust, reliable 3D grid generation**		**Improve usability of 3D simulators**			**Exploit parallel computation**	

** For 2001–2002, workarounds exist for the issues listed above, but research is still required for predictability*

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

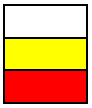

Table 103b Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
Overall technology cost reduction target (due to TCAD)	25%		35%			40%	
Lithography Modeling							
Resist profile prediction accuracy	10% (13nm)	10% (11.5nm)	10% (10nm)	10% (9nm)	10% (8nm)	10% (7nm)	10% (6.5nm)
OPC model accuracy	5% (6.5nm)	5% (5.8nm)	5% (5nm)	5% (4.5nm)	5% (4nm)	5% (3.5nm)	5% (3.3nm)
Front End Process Modeling							
Vertical junction depth simulation accuracy	5% (6.5nm)	5% (5.8nm)	5% (5nm)	5% (4.5nm)	5% (4nm)	5% (3.5nm)	5% (3.3nm)
Lateral junction depth simulation accuracy	5% (6.5nm)	5% (5.8nm)	5% (5nm)	5% (4.5nm)	5% (4nm)	5% (3.5nm)	5% (3.3nm)
Total source/drain series resistance (accuracy)	20%	20%	20%	20%	20%	20%	20%
Back end process/Equipment/Topography Modeling							
Etch/deposition cross wafer uniformity (% accuracy of the control spec)	10% (13nm)	10% (11.5nm)	10% (10nm)	10% (9nm)	10% (8nm)	10% (7nm)	10% (6.5nm)
2D/3D topography accuracy	10% (13nm)	10% (11.5nm)	10% (10nm)	10% (9nm)	10% (8nm)	10% (7nm)	10% (6.5nm)
Device modeling (Numerical)							
Accuracy of ft at given ft (% of maximum chip frequency)	10%	10%	10%	10%	10%	10%	10%
Gate leakage current accuracy (%) (I_g/I_{off})	70%	70%	40%	40%	40%	30%	30%
I_{on} accuracy	5%	5%	5%	5%	5%	3%	3%
I_{off} accuracy	70%	70%	40%	40%	40%	30%	30%
Long-channel V_t (accuracy)	4% (48–60mV)	3% (33–42mV)	3% (27–36mV)	3% (24–33mV)	3% (21–30mV)	3% (18–27mV)	3% (17–23mV)
V_t rolloff accuracy (mV)	20mV	20mV	15mV	15mV	15mV	10mV	10mV
V_t 3svariation (%)	30%	30%	30%	30%	30%	30%	30%
Circuit Element Modeling/ECAD							
I-V error—compact model accuracy	5%	5%	5%	5%	5%	3%	3%
Sub-threshold current accuracy model accuracy	50%	20%	10%	10%	10%	7%	7%
Intrinsic MOS C-V accuracy	<6%	<5%	<5%	<5%	<5%	<3%	<3%
Parasitic C-V accuracy	5–10%	5%	5%	5%	5%	<3%	<3%
Accuracy of Gm and r0 at V_t +150mV versus L, Vbs, Vds and T	20%	15%	10%	10%	10%	5%	5%
Circuit delay accuracy (% of maximum chip frequency)	5%	5%	5%	5%	5%	3%	3%
RLC delay accuracy (% of maximum chip frequency)	5%	5%	5%	5%	5%	3%	3%
Package Modeling							
Package delay accuracy (% of off-chip clock frequency)	1%	1%	1%	1%	1%	1%	1%
Temperature distribution for chip and package (accuracy)	5C	5C	5C	5C	5C	5C	5C
Numerical Methods							
Speed-up of algorithms for 3D process/device	2×	3×	4×	5×	6×	7×	8×
Linear solvers (kilo equations/minute)	250k	300k	600k	650k	700k	750k	800k
Parallel speed-up	2×	3×	4×	6×	8×	12×	16×
MFLOPS required	1000	2000	4000	5000	6500	8000	10000

** The accuracy numbers in the table are those expected after detailed calibration to experimental data.*

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

Table 103c Modeling and Simulation Technology Requirements: Capabilities—Long-term

Year of Production	*2010*	*2013*	*2016*
DRAM ½ PITCH (nm)	*45*	*32*	*22*
MPU / ASIC ½ PITCH (nm)	*50*	*35*	*25*
Lithography Modeling			
Next generation lithography	NGL models		
Resist technology	Finite polymer-size effects	Non-conventional photo-resist models	
Front End process Modeling			
Advanced process models	Alternative materials	Atomistic process model	
Advanced doping models	New technology needed		
Back End process/Equipment/Topography Modeling			
Alternative material models	Calculation of dielectric constant	Atomistic material model- materials to electronic properties	
Equipment simulation	Computer engineered materials and process recipes		
Numerical Device Modeling			
Emerging devices	Trade-off analysis tools	Quantum effect devices	
Circuit Element Modeling/ECAD			
Advanced circuit models	Circuit models for alternative devices	New technology needed	
Package Modeling			
Electrical/optical models	Mixed electrical/-optical analysis	New technology needed	
Numerics			
Numerical algorithms	Efficient atomistic/ quantum methods	Multi-scale simulation (atomistic-continuum)	

White—Manufacturable Solutions Exist, and Are Being Optimized
Yellow—Manufacturable Solutions are Known
Red—Manufacturable Solutions are NOT Known

SUMMARY

Modeling and Simulation software tools span the entire semiconductor world. These tools are being used daily more and more effectively. This document has presented specific needs to increase this effectiveness and provide impact on our industry in the future.

Besides specific technical needs, the Modeling and Simulation community recommends effort in several non-technical areas that would dramatically help this field.

- Increase cross-discipline efforts that bring in experts from non-traditional fields to aid in solving the difficult challenges.
- Adequately support research funding at universities and laboratories for directed long range research.
- Explore ways of standardizing and/or opening up some of the universally used Modeling and Simulation modules so that the focus of new efforts can be in value-add areas.
- Improve the methodologies for evaluating the impact of Modeling and Simulation.
- Ensure that a hierarchy of software tools are developed and used—from spreadsheet to *ab-initio*.
- Explore ways for the equipment suppliers to provide physical models and modeling information with equipment.

REFERENCES AND RESOURCES

Other information regarding future Modeling and Simulation for semiconductor processing are available through *supplemental material discussing nanoelectronics, the Technology Roadmap for Nanoelectronics*[2] produced by the European Commission's IST programme (Future and Emerging Technologies). Also, the working group received contributions to this discussion from the European ESPRIT Industrial User Group "UPPER," funded by the European Commission [see http://www.iis-b.fhg.de/en/arb_geb/upper.htm].

[2] *R. Compano, ed. Technology Roadmap for Nanoelectronics. Second Edition. November 2000.*