INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2011 EDITION

METROLOGY

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METROLOGY

1. INTRODUCTION AND SCOPE

1.1. INTRODUCTION

Metrology is defined as the science of measurement. The ITRS Metrology Roadmap describes new challenges facing metrology and describes a pathway for research and development of metrology with the goal of extending CMOS and accelerating Beyond CMOS. Metrology also provides the measurement capability necessary for cost-effective manufacturing. As such, the metrology chapter of the ITRS focuses on difficult measurement needs, metrology tool development, and standards.

The roadmap for feature size reduction drives the timeline for metrology solutions for new materials, process, and structures. Metrology methods must routinely measure near and at atomic scale dimensions which require a thorough understanding of nano-scale materials properties and of the physics involved in making the measurement. Novel materials and geometries, such as 3D gates and strained silicon channels, add to the complexity of measurements. Metrology development must be done in the context of these issues. Metrology enables tool improvement, ramping in pilot lines and factory start-ups, and improvement of yield in mature factories. Metrology can reduce the cost of manufacturing and the time-to-market for new products through better characterization of process tools and processes. The increasing diversity of chip types will spread already limited metrology resources over a wider range of challenges. The metrology community including suppliers, chip manufacturers, consortia, and research institutions must provide cooperative research, development, and prototyping in order to meet the ITRS timeline.

The lack of certainty in the structures and materials of future technology generations makes the definition of future metrology needs less clear than in the past. However, it is clear that 3D device structures will be introduced by at least some companies as early as the 22 nm node. Such 3D device structures invalidate many of the starting assumptions for the modeling and analyses of conventional metrologies necessitating an increased emphasis on metrology techniques which can provide true 3D information. The 3D nature of both front end and interconnect devices and structures provides many challenges for all areas of metrology including critical dimensions. Although advancements in materials characterization methods, such as aberration corrected transmission electron microscopy, have achieved atomic resolution for 2D materials, including single layer graphene, critical dimension measurement with nm level precision is difficult to achieve particularly for 3D structures. Feature shape characterization and metrology done largely in 2D will need to evolve to 3D. The 2011 ITRS expands on the new urgency for Metrology for 3D Interconnects to include wafer alignment, interface bonding, and through silicon vias (TSV).

Moreover, it is entirely possible that different materials will be used by different manufacturers at a given technology generation, potentially requiring different metrologies. In the near term, advances in electrical and physical metrology for high- and low-κ dielectric films must continue. The strong interest in EUV Lithography is driving the need for new mask metrology. The requirement for technology for measurement of devices on ultra-thin and possibly strained silicon on insulator comes from the best available information that is discussed in the *Front End Processes* Roadmap. The increasing emphasis on active area measurements instead of test structures in scribe (kerf) lines places new demands on metrology. Measurement of relevant properties, such as stress or strain, in a nano-sized, buried area such as the channel of a small dimension gate is a difficult task. Often, one must measure a film or structure property at the surface and use modeling to determine the resultant property of a buried layer. Long-term needs at the sub-16 nm technology generation are difficult to address due to the lack of clarity of device design and interconnect technology. The selection of a replacement for copper interconnect remains a research challenge. Although materials characterization and some existing inline metrology apply to new device and interconnect structures, development of manufacturing capable metrology requires a more certain knowledge of materials, devices, and interconnect structures. The 2011 ITRS also includes the addition of a MEMS chapter.

Metrology tool development requires access to new materials and structures if it is to be successful. It requires state-of-the-art capabilities to be made available for fabrication of necessary standards and development of metrology methodologies in advance of production. The pace of feature size reduction and the introduction of new materials and structures challenge existing measurement capability. In some instances, existing methods can be extended for several technology generations. In other cases, necessary measurements may be done with inadequate equipment. Long-term research into nano-devices may provide both new measurement methods and potential test vehicles for metrology. A

greater attention to expanding close ties between metrology development and process development is needed. When the metrology is well matched to the processes and process tools, ramping times for pilot lines and factories are reduced. An appropriate combination of well-engineered tools and appropriate metrology is necessary to maximize productivity while maintaining acceptable cost of ownership.

The fundamental challenge for factory metrology will be the measurement and control of atomic dimensions while maintaining profitable high volume manufacturing. In manufacturing, metrology is connected to factory-wide automation that includes database and intelligent information from data capability. Off-line materials characterization is also evolving toward compatibility with factory-wide automation. All areas of measurement technology (especially those covered in the *Yield Enhancement chapter)* are being combined with computer integrated manufacturing (CIM) and data management systems for information-based process control. Although integrated metrology still needs a universal definition, it has become the term associated with the slow migration from offline to inline and *in situ* measurements. The proper combination of offline, inline, and *in situ* measurements will enable advanced process control and rapid yield learning.

The expected trend involves the combined use of modeling with measurement of features at the wafer surface. *The Metrology roadmap has repeated the call for a proactive research, development, and supplier base for many years*. The relationship between metrology and process technology development needs fundamental restructuring. In the past the challenge has been to develop metrology ahead of target process technology. Today we face major uncertainty from unresolved choices of fundamentally new materials and radically different device designs. *Understanding the interaction between metrology data and information and optimum feed-back, feed forward, and real-time process control are key to restructuring the relationship between metrology and process technology.* A new section has been added to the Metrology Roadmap that covers metrology needs for emerging technology paradigms.

1.2. Scope

The metrology topics covered in the 2011 *Metrology* roadmap are microscopy; critical dimension (CD) and overlay; film thickness and profile; materials and contamination analysis; 3D metrology; emerging research materials and devices; and reference materials. These topics are reported in the following sections in this chapter: Microscopy; Lithography Metrology; Front End Processes Metrology; 3D Interconnect Metrology; Traditional Interconnect Metrology; Materials and Contamination Characterization; Metrology for Emerging Research Materials Devices; Reference Materials; and Reference Measurement Systems.

International cooperation in the development of new metrology technology and standards will be required. Both metrology and process research and development organizations must work together with the industry including both the supplier and IC manufacturer. Earlier cooperation between IC manufacturers and metrology suppliers will provide technology roadmaps that maximize the effectiveness of measurement equipment. Research institutes focusing on metrology, process, and standards; standards organizations; metrology tool suppliers; and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials. Despite the existence of standardized definitions and procedures for metrics, individualized implementation of metrics such as measurement precision to tolerance (P/T) ratio is typical.[1] The P/T ratio is used to evaluate automated measurement capability for use in statistical process control and relates the measurement variation (precision) of the metrology cluster to the product specification limits. Determination of measurement tool variations is sometimes carried out using reference materials that are not representative of the product or process of interest. Thus, the measurement tool precision information may not reflect measurement-tool induced variations on product wafers. It is also possible that the sensitivity of the instrument could be insufficient to detect small but unacceptable process variations. There is a need for metrics that accurately describe the resolution capability of metrology tools for use in statistical process control. The inverse of the measurement precision-to-process variability is sometimes called the signal-to-noise ratio or the discrimination ratio. However, because the type of resolution depends on the process, specific metrics may be required (e.g. thickness and width require spatial resolution while levels of metallic contaminants on the surface require atomic percent resolution). There is a new need for a standardized approach to determination of precision when the metrology tool provides discrete instead of continuous data. This situation occurs, for example, when significant differences are smaller than the instrument resolution.

The principles of integrated metrology can be applied to stand-alone and sensor-based metrology itself. Factors that impact tool calibration and measurement precision such as small changes in ambient temperature and humidity could be monitored and used to improve metrology tool performance and thus improve statistical process control.

Wafer manufacturers, process tool suppliers, pilot lines, and factory start-ups all have different timing and measurement requirements. The need for a shorter ramp-up time for pilot lines means that characterization of tools and processes prior to pilot line startup must improve. However, as the process matures, the need for metrology should decrease. As device

dimensions shrink, the challenge for physical metrology will be to keep pace with inline electrical testing that provides critical electrical performance data.

1.3. INFRASTRUCTURE NEEDS

A healthy industry infrastructure is required if suppliers are to provide cost-effective metrology tools, sensors, controllers, and reference materials. New research and development will be required if opportunities such as MEMS-based metrology and nanotechnology are to make the transition from R&D to commercialized products. Many metrology suppliers are small companies that find the cost of providing new tools for leading-edge activities prohibitive. Initial sales of metrology tools are to tool and process developers. Sustained, high-volume sales of the same metrology equipment to chip manufacturers do not occur until several years later. The present infrastructure cannot support this delayed return on investment. Funding that meets the investment requirements of the supplier community is needed to take new technology from proof of concept to prototype systems and finally to volume sales.

2. DIFFICULT CHALLENGES

Metrology requirements continue to be driven by advanced lithography processes, new materials, and Beyond CMOS materials, structures, and devices. The push for EUV Lithography is driving the development of new metrology equipment for masks. Existing Critical Dimension metrology is approaching its limits and requires significant advances to keep pace with the needs of patterning. Another key challenge to critical dimension metrology is tool matching. Near term precision (measurement uncertainty) requirements for the next few years can be met using single tools. Overlay metrology capability lags behind the need for improved overlay control. Front end processes continue to drive metrology to provide measurements for new channel materials including III-V film stacks, higher dielectric constant materials, dual work function metal gates, and new ultra shallow junction doping processes. 3D device structures such as FinFETs place significantly more difficult requirements on dimensional and doping metrology. The need for porosity control for low k materials has driven a renewed interest in porosity measurements. 3D interconnect metrology requirements are largely driven by the activity in through silicon vias (TSV) R&D. Bonded wafer overlay control for next generation. Potential solutions for bonded wafer overlay are now available. For Beyond CMOS R&D, many areas of graphene metrology have advanced but putting them into volume manufacturing will require challenging R&D. The need for understanding large area graphene uniformity is driving both physical and electrical metrology. In addition, metrology R&D is working with other Beyond CMOS materials.

2.1. DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 16 nm ½ pitch Metrology needs after 2019 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table MET1 presents the ten major challenges for metrology. Table MET2 presents the technology requirements for Metrology.

Table MET1 Metrology Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Directed Self Assembly Lithography, complicated 3D structures such as FinFET & MuGFET transistors, capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Although there have been significant advances in off-line characterization of FinFET structures, the recent announcement that a FinFET transistor will be used in manufacturing at the 16 nm 1/2 pitch has placed renewed emphasis on the near term need for in-line metrology for dimensional, compositional, and doping measurements. The materials properties of block co-polymers result in new challenges for lithogrpahy metrology. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 16 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-16 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for ***beyond CMOS.***	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

Table MET2 Metrology Technology Requirements

3. MICROSCOPY

Microscopy is used in most of the core technology processes where two-dimensional distributions, that is digital images of the shape and appearance of integrated circuit (IC) features, reveal important information. Usually, imaging is the first, but many times the only step in the “being able to see it, measure it, and control it” chain. Microscopes typically employ light, electron beam, or scanned probe methods. Beyond imaging, online microscopy applications include critical dimension (CD) and overlay measurements along with detection, review, and automatic classification of defects and particles. Because of the high value and quantity of wafers, the need for rapid, non-destructive, inline imaging and

measurement is growing. Due to the changing aspect ratios of IC features, besides the traditional lateral feature size (for example, linewidth measurement) full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques, telepresence, and networked measurement tools will be needed to meet the requirements of near future IC technologies. Microscopy techniques and measurements based on them must serve the technologists better giving fast, detailed, adequate information on the processes in ways that help to establish process control in a more automated manner.

For all types of microscopy and for the metrology based on them it is becoming increasingly important to develop and provide reliable and easy-to-use methods that monitor the performance of the instruments. Due to the small sizes of the integrated circuit structures these instruments must work at their peak performance, which is not easy to attain and sustain. Currently only rudimentary methods are available to ensure adequate performance. Beyond imaging and measurement resolution, a host of other, tool-dependent parameters also need to be regularly monitored and optimized. These key parameters have significant influence on the results, and it is indispensable to include their contribution in the uncertainty statements of the measurements.

Electron Microscopy—There are many different microscopy methods that use electron beams as sources of illumination. These include scanning electron microscopy, transmission electron microscopy, scanning transmission electron microscopy, electron holography, and low-energy electron microscopy. Scanning electron microscopy and electron holography are discussed below, and transmission electron microscopy, scanning transmission electron microscopy, and low-energy electron microscopy are discussed in the section on Materials and Contamination Characterization.

Scanning Electron Microscopy (SEM)—continues to provide at-line and inline imaging for characterization of cross-sectional samples, particle and defect analysis, inline defect imaging (defect review), and CD measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 32 nm generation. New inline SEM technology, such as the use of ultra-low-energy electron beams (< 250 eV) and high energy SEM (10keV-200keV) may be required for overcoming image degradation due to charging, contamination, and radiation damage of the sample surface, while maintaining adequate resolution and depth of field. Improving the resolution of the SEM by the reduction of spherical aberration leads to an unacceptably small depth of field and SEM imaging with several focus steps and/or use of algorithms that take the beam shape into account might be needed. Aberration correction lens technology has migrated from transmission electron microscopy to SEM providing a significant increase in capability. Other non-traditional SEM imaging techniques, such as the implementation of nano-tips and electron holography, need further development to be production-worthy methodologies. A new alternative path could be high-pressure or environmental microscopy, which opens the possibility for higher accelerating voltage, high-resolution imaging, and metrology. Binary and phase-shifting chromium-on-quartz optical photomasks have been successfully investigated with this mode of high-resolution scanning electron microscopy. It has been found that the gaseous sample environment minimizes sample charging and contamination. This methodology also holds promise for the inspection, imaging, and metrology of wafers.

Data analysis methods that adhere to the physics of the measurement and use all information collected were demonstrated to be better than arbitrary methods.[1] Measured and modeled image and fast and accurate comparative techniques are likely to gain importance in SEM dimensional metrology. A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement. Sample damage, which arises from direct ionization damage of the sample and deposition of charge in gate structures, may set fundamental limits on the utility of all microscopies relying on charged particle beams. Shrinkage, another form of damage often caused by electron beams on polymer layers, including photoresists, is now better understood and in many cases can now be predicted and compensated for in CD measurement values. [1]

Determination of the real 3D shape for sub-90 nm contacts/vias, transistor gates, interconnect lines, or damascene trenches will require continuing advances in existing microscopy and sample preparation methods. Fully automated cross-sectioning by FIB and semi-automated lift-out for imaging in a TEM or a STEM has been successfully demonstrated.

He Ion Microscopy (HIM)—has been proposed as a means of overcoming the issues associated with the spread in effect probe size due to the interaction of finely focused electron beams and the sample. Potential applications of this technology include CD, defect review, and nanotechnology. Sub-1nm resolution by HIM has been achieved, but sample interaction questions are as yet unanswered. For IC manufacturing metrology, current thoughts are that HIM needs to be able to fill a key gap, the imaging of high aspect ratio etched contact holes and trenches without causing too much damage, to secure its place as an in-line workhorse wafer metrology solution.

Scanning Probe Microscopy (SPM)—may be used to calibrate CD-SEM measurements. Stylus microscopes, such as the atomic force microscope (AFM), offer 3D measurements that are insensitive to the material scanned. Flexing of the stylus degrades measurements when the probe is too slender. The stylus shape and aspect ratio must, therefore, be appropriate for the probe material used and the forces encountered. High stiffness probe materials, such as short carbon nano-tubes, may alleviate this problem. Other types of scanning probe microscopy are discussed in the metrology for Emerging Research Materials and Devices section.

Far-field Optical Microscopy—is limited by the wavelength of light. Deep ultraviolet sources and near-field microscopy are being developed to overcome these limitations. Improved software allowing automatic classification of defects is needed. Optical microscopes will continue to have application in the inspection of large features, such as solder bump arrays for multi-chip modules. Also, other new experimental optical applications that move beyond directly measuring from images have potential to allow for measurement of smaller features for measurements or for process excursion flagging, but more work is needed to understand if they have a place for in-line metrology. [2],[3,]

For *defect detection*—each technology has limitations. A defect is defined as any physical, electrical, or parametric deviation capable of affecting yield. Existing SEMs and SPMs are considered too slow for the efficient detection of defects too small for optical microscopes. High-speed scanning has been demonstrated with arrayed SPMs, (that might be faster than SEMs) but issues associated with stylus lifetime, uniformity, characterization, and wear need to be addressed. This technology should be pursued both by expanding the size of the array and in developing additional operational modes. Arrayed micro-column SEMs have been proposed as a method of improving SEM throughput and operation of a single micro-SEM has been demonstrated. Research is needed into the limits of electrostatic and magnetic lens designs.

4. LITHOGRAPHY METROLOGY

Lithography metrology continues to be challenged by rapid advancement of patterning technology. New materials in all process areas add to the challenges faced by Lithography metrology. A proper control of the variation in transistor gate length starts with mask metrology. Although the overall features on a mask are four times larger than as printed, phase shift and optical proximity correction features are roughly half the size of the printed structures. Indeed, larger values for mask error factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology has to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimension and overlay are also becoming more challenging. CD control for transistor gate length continues to be a critical part of manufacturing ICs with increasing clock speeds. The metrology needs for process control and dispositioning of product continue to drive improvements in measurement uncertainty. Acceleration of research and development activities for CD and overlay measurement are essential if we are to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability. (Refer to the *Lithography chapter*.)

On-product monitors of effective dose and focus extend utility of conventional microscopy-based CD metrology systems in process control applications. The same system can output CD and overlay measurements, as well as lithography process monitors. Process control capability and efficiency of such metrology are improving. The infrastructure to support such new applications is generally available. Monitors of effective dose and focus for lithography process control have also been developed for conventional optical metrology systems, such as used in overlay metrology. Similar capabilities, in addition to CD, sidewall, and height metrology, are now emerging in scatterometry. In all cases, rather than measure CD for the purpose of process control, with every feature's CD being a complex function of both dose and focus, these systems output measurements of process parameters themselves, with metrology errors as low as 1% (3 σ) for dose and ~10 nm (3 σ) for focus. Today's process monitor performance levels boast P/T = 0.1 for lithography process window with 15% for dose and 200 nm for focus, enabling further reduction of k_1 in high volume manufacturing and extending the utility of optical microlithography. While the demands on metrology systems' stability and matching are likely to increase[6], work in this area has already initiated the development of tighter control and matching, being a pre-requisite of accurate CD metrology, not just of process control applications and dedicated process monitors.

Capable and efficient direct process monitor-based lithography process control has the potential to overcome technology limitations of conventional CD metrology. The ongoing change of lithography process control methodology can be accelerated by industry collaboration to define the expectations in direct process control, with tests of performance and standards for both new metrology applications and applications environment. This change will, likely, result in the lithography metrology where capable and efficient means of process control are supplemented by, and are differentiated from, superior critical dimension metrology proper. New levels of absolute accuracy are required to meet measurement requirements for next generation technology especially in the areas of CD metrology for calibration and verification of

compliance for advanced mask designs (for example, 1-D and 2-D/3-D CD metrology through pitch and layouts, in presence of OPC and RET, at various printing conditions).

There is no single metrology method or technique that can deliver all needed information. Therefore, in order to be able to compare the results of various dimensional metrology tools and methods meaningfully, parameters beyond repeatability and precision need to be addressed. Each measurement application requires consideration of the need for relative accuracy (sensitivity to CD variation and insensitivity to secondary characteristic variation), absolute accuracy (traceability to absolute length scale), LER and sampling, and the destructive nature of the measurement.

It would be ideal to have all metrology tools properly characterized for measurement uncertainty including a breakout of the leading contributors to this uncertainty. It is recommended to use internationally accepted methods to state measurement uncertainty. This knowledge would help to make the most of all metrology tools, and it would prevent situations in which the measured results do not provide the required information. Finally, once the largest contributors to measurement errors are known, a faster development of better instruments could take place. It is now recommended to state the measurement uncertainty of various dimensional metrology tools according to internationally accepted methods and to identify (quantify) the leading contributors.[7] Another possibility is the combination of information from multiple metrology techniques into "hybrid metrology", where separate, different dimensional metrology tools not only are calibrated together but can either communicate to each other to share extra information to improve each other's uncertainties and rectify inter-variable correlations. [4]

Often, special test structures are measured during manufacturing. When this is the case, active device dimensions are not measured. CD-SEM continues to be used for wafer and mask measurement of lines and via/contact. A considerable effort has been aimed at overcoming electron beam damage to photoresist used by 193 nm exposures[8] and that will continue when alternative lithography techniques, like EUV, are introduced; as discussed above in the microscopy section, these efforts are starting to yield real results. Stack materials, surface condition, line shape, and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects, unless they are accurately modeled and corrected, increase measurement variation and total uncertainty of CD-SEM measurements. Developments in electron beam source technology that improve resolution and precision are being tested. CD-SEM is facing an issue with poor depth of field unless a new approach to SEM-based CD measurement is found. High-voltage CD-SEM and low loss detectors have been proposed as means of extending CD-SEM.

To be able to make statistically sound SEM measurements it is essential to collect the right kind and amount of information. The collection of excess information leads to loss of throughput, and by the contrary, collection of not enough or of the wrong type of information leads to loss of process control. It is important to develop metrology methods that reveal and express the needed information with the indication of the validity of the measurements. Larger usable image field-of-view at image resolution-level pixel density allows for much greater utilization of multiple feature measurement (MFM) applications for increased information per unit time, and thus improved validity of measurement results, through increased sampling without throughput penalty.

For CD-SEMs, Design-Based Metrology (DBM) applications, which include automatic recipe setup from design information, allow for practical use of SEMs for large-scale verification of design intent, through the collection of feature 2D contour shape information and comparison to GDS files. DBM applications are becoming very important for development and verification of lithographic optical proximity corrections (OPC), as the number of measurements for successfully developing OPC is expected to grow exponentially with technology generation. Also, DBM applications for Double Patterning are being explored. This is a major role where metrology interfaces with the Design for Manufacturing (DFM) community. Also, collecting and applying CD information from reticle measurements for comparison to wafer CD measurements is an important application in some cases, and would be most efficient if done through contours.

However, much work remains to be done in defining contour error source testing methodologies, contour reference metrology, and SEM modeling for contours[11] [12] [13]. Contour fidelity is a prevailing challenge and an area where improvements in the state of the art could yield value to the industry. Gaps or missing segments in contours can occur for reasons related to both the sample and metrology tool. Major contributors are weak signal and breaks along edges parallel to the (fast) scan axis and contrast variation along the contour, which could be due to underlying variations in the structure (e.g., changes in sidewall angle or reentrance) or instrumental artifacts, such as edge proximity effects in an scanning electron microscope (SEM). In some cases, breaks in the contour are inherent when referencing one level to another (e.g., poly over active). This subject of contour integrity is closely related to the accuracy of contour extraction. Contour extraction algorithms employ 2-D image processing and thus function differently than conventional single-measurand critical dimension (CD) extraction algorithms, which are applied to individual line scans. There are known significant differences specifically with regard to edge detection and the inherent degree of signal averaging. Sampling

can also have a large impact, as averaging as few as five contours can significantly improve precision and, due to averaging out local roughness effects in discrete features, also improve agreement between extracted contours and simulation.

Attention must also be paid to the requirements for registration between the SEM contours and the design for successful OPC. Models must be able to compensate for rotational and lateral offsets between the SEM contour and the design, as well as for potential field distortions. This relates somewhat to the question of metrology accuracy versus production accuracy. The extent to which it is acceptable to remove metrology errors when matching contours to the design is not agreed upon. For example, a uniform magnification error removed by stretching the contour could be less problematic than non-linearity across the SEM field of view.

Another area in which useful improvements could be made in contour metrology accuracy lies in the statistical sophistication of the contour extraction and modeling software, for example, the inclusion of a 95 % confidence interval for the extracted contour. It should be noted that the final metrics in measuring contours should be compatible with the same conventional linewidth metrics used in this roadmap.

Scatterometry has moved into manufacturing, and does provide line shape metrology. Scatterometry refers to both single wavelength—multi angle optical scattering and to multi-wavelength—single angle methods. Recent advances have resulted in the ability to determine CD and line shape without the aid of a library of simulated results. Scatterometry has already been shown to provide a tighter distribution of key transistor electrical properties when used in an advanced process control mode. One next step is the development of scatterometry for contact and via structures, and for features with complexity which require many parameters to model. Scatterometry models assume uniform optical property of line and background materials. Surface anomalies and non-uniform dopant distribution may affect scatterometry results. Therefore, scatterometry models need calibration and periodic verification. Lithography and etch microloading effects may noticeably affect line CD. Since scatterometry makes measurements on special test structures, other CD metrology techniques (such as SEM, AFM, or TEM) need to be employed to establish correlation between CD of the scatterometry structure and CDs of the circuit. Scatterometry needs to be capable of measuring smaller test structures while improving measurement precision. The increasing usage of double patterning may create some issues in measurement of double-patterned features, as many more parameters must be measured and controlled, potentially including two statistically distinct CD, sidewall, roughness, and pitch (overlay) populations. In some schemes, an ARC may prevent the UV light from penetrating deeper layers.

New CD measurement methods have been proposed, and it seems likely the first opportunity for them to move into manufacturing is at the 16 nm DRAM half pitch. The 22 nm half pitch is already well into the development stage and beta equipment is available for all process areas. The new potential solutions include the He ion microscope (discussed in the microscopy section) and small angle x-ray scattering (CD-SAXS). Using transmission measurements and a grating structure, CD-SAXS has shown the ability to measure average CD, sidewall roughness, and CD variation from an individual line in a grating structure, and for more complex lines through multiple layers.

The use of “feed forward” control concepts must be extended to lithography metrology taking data at least from resist and mask measurements and controlling subsequent processing, such as etch, to improve product performance. “Feed back” controlling strategy is required as well to set properly process parameter setup from a huge amount of previously collected data. The use of overlay measurement equipment for CD control has also been reported. This method is based on the fact that the change in line width also affects the length of the photoresist lines that can then be measured using the optical microscope of the overlay system. A special test structure with arrays of line and arrays of spaces is required.

CD-AFM measurements can be used to verify line shape and calibrating CD or contour measurements. New probe tip technology and 3-D tiltable cantilever is required if CD-AFM is to be applied to dense line measurement below 50 nm. Focus–Exposure correlation studies (especially for contact/via) can be using all of the above methods as well as by the dual column FIB (SEM plus Focused Ion Beam) where there is an immediate correlation with line shape. Electron holography has been proposed as a long term CD measurement technology.

At some upcoming technology node, some say 16 nm, the bulk of logic manufacturing will leave the simpler realm of planar devices and move to non-planar architectures such as FimFETs, and a similar transition for memory architecture is already imminent. This will cause many new issues to metrology, where the main variables for process control may not be the bottoms of profiles. Thus, truly 3D metrology with great sensitivity will be required.

4.1. LINE ROUGHNESS

Line edge roughness (LER) is an important part of lithography process control, and line width roughness (LWR) is an important part of etch process control. The Lithography Roadmap provides metrics for both LER and LWR. LWR

correlates to an increase in transistor leakage current but not to changes in drive current. LER and LWR are determined per the SEMI standard definition.[15] It is important to note that the precision requirements for LER and LWR are several years ahead of those required for CD as indicated below. CD-SEM and lithography process simulation systems have software that determines LER and LWR, but not all systems yet adhere to the SEMI standard for LER and LWR measurement.

LER/LWR is evaluated by two methods: spectral analysis and measurement of LER/LWR amplitude/degree (generally, 3 σ of residuals from average position or average CD). Fourier spectrum of LER/LWR is becoming popular in R&D; however, 3 σ is still the most useful index for practical in-line metrology. In evaluating LER/LWR, length of the inspected edge, L, and sampling interval of edge-detection, Δy, are the most important measurement parameters because 3 σ strongly depends upon these values.

The recommended LER/LWR metric is thus defined as the 3σ of residuals measured along 2- μ m-long line for the present; however, transistor performance could be more sensitive against in-gate roughness in the future. In that case, a new index for in-gate roughness (such as high-frequency LWR) should be additionally defined. To evaluate LWR-caused gate-CD variation separately, low-frequency LWR index should also be defined.

Another important factor in measurement of LWR/LER on imaging tools is edge detection noise. This noise has the effect of adding a positive bias to any roughness measurement. This is shown by the equation $LWR_{meas}^2 = LWR_{actual}^2 + \sigma_\varepsilon^2$ where LWR_{meas} is the measured value, LWR_{actual} is the actual roughness of the target, and σ_ε is the noise term, defined as the reproducibility of locating an edge along one single sampling point. The size of σ_ε has been measured to be on the order of 2 nm, which means that at future technology generations this measurement artifact could mask the actual roughness to be measured. A methodology has been demonstrated to remove this noise term, leading to an unbiased estimation of the roughness. Use of this is deemed very important to ensuring accuracy of roughness measurement in the future, and should be a key ingredient in allowing for intercomparison of data across the litho-metrology community. It should be noted that LWR metrology becomes more challenging when the resolution of the metrology tool becomes close to the LWR requirement. At the 22 nm node the LWR required is 1.3 nm. Current CD-SEM equipment has comparable resolution performance.

4.2. Measurement Uncertainty

Critical dimension measurement capability does not meet uncertainty requirements that comprehend measurement variation from individual tool reproducibility, tool-to-tool matching and sample-to-sample measurement bias variation. Precision is defined by SEMI as a multiple of reproducibility. Reproducibility includes repeatability, variation from reloading the wafer, and long-term drift. In practice, reproducibility is determined by repeated measurements on the same sample and target over an extended period of time. Although the precision requirements for CD measurement in the ITRS have always included the effects of line shape and materials variation, repeated measurements on the same sample would never detect measurement uncertainty related to sample-to-sample bias variation. Therefore, with the current methodology the uncertainty of measurement associated with variation of line shape, material, layout, or any other parameters will not be included in the precision. Typically, reference materials for CD process control are specially selected optimum or “golden” wafers from each process level. Thus, industry practice is to determine measurement precision as a reproducibility of the measurement for each process level. The measurement bias is not detected. This approach misses measurement bias variation component of measurement uncertainty. In light of this, a metric, total measurement uncertainty (TMU) can be used. The TMU is determined using a technology representative set of samples that accounts for variations in measurement bias associated with each process level. This idea can be extended to use with a production fleet of tools through another metric Fleet Matching Precision (FMP). These metrics assume accuracy for all tools, and that a fleet of tools behave as well as a single tool would be required. It should be noted that other metrics for accuracy and matching are also available.

Calibration of inline CD metrology equipment requires careful implementation of the calibration measurement equipment referred to as reference metrology. For example, laboratory based TEM or CD-AFM must have precision that matches or exceeds inline CD and have to be frequently calibrated. Reference materials used during manufacturing must be representative to the actual process level and structure and reflect the pertinent process variations to be evaluated by the tool under test. Reports of this approach already exist.

CD measurement has been extended to line shape control. Tilt beam CD-SEM, comparison of line scan intensity variation versus line scans from a golden wafer, scatterometry, CD-AFM, dual beam (electron and gallium ion beam systems) and triple beam (electron, Gallium ion beam and Argon ion beam systems) have all been applied to line shape measurement. Sidewall angle has been proposed as the key process variable. Already, photoresist lines have shapes that are not well described by a single planar description of the sidewall. Line edge and line width roughness along a line, vertical line

edge roughness, and rounded top shapes are important considerations in process control. As mentioned above, precision values change with each process level. This adds to the difficulty in determination of etch bias (the difference in CD before and after etch). Electrical CD measurements provide a monitoring of gate and interconnect line width, but only after the point where reworking the wafers is no longer possible and does not allow a real-time correction of process parameter. Electric CD measurements are limited in their applicability to conducting samples.

Mask metrology is moving beyond the present optical technology. Binary and phase-shifting chromium on quartz optical photomasks have been successfully investigated with high-pressure/environmental scanning electron microscopy. Environmental SEM instrumentation equipped with high-resolution, high-signal, field emission technology in conjunction with large chamber and sample transfer capabilities are in use in the semiconductor industry for mask CD. The high-pressure SEM methodology employs a gaseous environment to help to compensate for the charge build-up that occurs under irradiation with the electron beam. Although potentially very desirable for the charge neutralization, this methodology has not been seriously employed in photomask or wafer metrology until now. This is a new application of this technology to this area, and it shows great promise in the inspection, imaging, and metrology of photomasks in a charge-free operational mode. This methodology also holds the potential of similar implications for wafer metrology. For accurate metrology, high-pressure SEM methodology also affords a path that minimizes, if not eliminates, the need for charge modeling.

Lithography metrology consists not only of overlay and CD metrology, but also includes the process control and characterization of materials needed for lithography process, especially photoresists, phase shifters, and antireflective coatings (ARCs). As these lithography materials become more complex, the materials characterization associated with them also increases in difficulty. Additionally, most non-lithography materials used in the wafer fabrication process (gate oxides, metals, low-κ dielectrics, SOI substrates) enter the lithography process indirectly, since their optical properties affect the reflection of light at a given wavelength. Even a small variation in process conditions for a layer not normally considered critical to the lithography process (such as the thickness of the buried oxide in SOI wafers) can change the dimensions or shapes of the printed feature, if this process change affected the optical response of the layer.

As a minimum, the complex refractive index (refractive index n and extinction coefficient κ) of all layers needs to be known at the lithography wavelength. Literature data for such properties are usually not available or obsolete and not reliable (derived from obsolete reflectance measurements on materials of unknown quality followed by Kramers-Kronig transform). In ideal cases, n and κ can be measured inline using spectroscopic ellipsometry at the exposure wavelength. Especially below 193 nm, such measurements are very difficult and usually performed outside of the fab by engineering personnel. EUV optical properties can only be determined using specialized light sources (such as a synchrotron or a EUV source for a EUV litho tool). Therefore, materials composition is often used as a figure of merit, when direct measurement of the optical properties is not practical. But even two materials with the same composition can have different optical properties (take amorphous and crystalline Si as an example).

Additional complications in the determination of the optical properties of a material arise from surface roughness, interfacial layers, birefringence, or optical anisotropy (often seen in photoresists or other organic layers responding to stress), or depth-dependent composition. For some materials for a wafer fab, it is impossible to determine the optical properties of such material, since the inverse problem of fitting the optical constants from the ellipsometric angles is underdetermined. Therefore, physical materials characterization must accompany the determination of optical properties, since physical characteristics, materials properties, and optical constants are all inter-related.

Overlay measurements are challenged by phase shift masks (PSM) and optical proximity correction (OPC) masks, and the use of different exposure tools and/or techniques for different process layers will compound the difficulty. Future overlay metrology requirements, along with problems caused by low contrast levels, will drive the development of new optical or SEM methods along with scanning probe microscopy (SPM). The need for new target structures has been suggested as a means of overcoming the issues associated with phase shift mask and optical proximity mask alignment errors not detectable with traditional targets. Overlay for on-chip interconnect will continue to be challenging. The use of chemical mechanical polishing for planarization degrades target structures. Thus as requirements for tighter overlay control are introduced, the line edge of overlay targets in interconnect are roughened. The low-κ materials used as insulators will continue to make overlay more difficult especially as porous low κ move into manufacturing.

The dramatic tightening of the overlay budget up to 20% [or 25%] of the device half-pitch, required for advanced applications in DRAM and NVM, calls for a faster introduction of alternative measuring solutions, like high-voltage SEM and scatterometry techniques, which are still far from being mature enough today, and may require breakthroughs also in metrology integration.

The introduction of EUV lithography requires further development in the area of EUV mask metrology and EUV Aerial Image Measurements Systems (EUV AIMS).

The Lithography Metrology Requirements Tables are divided into wafer and mask requirements Tables MET3, and MET4a and MET4b, respectively. The mask metrology requirements in Tables MET4a and MET4b are further divided into the needs for each type of exposure technology: optical, EUV, and electron projection.

4.3. Explanation Of Uncertainty In Tables MET3 And MET4

The preceding concepts are summarized by the following consideration for the precision of patterning metrology: the definition for precision critically depends on the application. Given the application and the metrology instrument, a sampling plan needs to be defined. The precision specification needs to be interpreted in light of application, instrument, and sampling plan. The application defines the accuracy, single tool precision, and matching requirements. In some applications, the relative accuracy and single tool precision are paramount. In some applications, tool matching and single tool precision are paramount. In some applications, a single measurement event is not sufficient to provide the needed measurement; rather the average of multiple measurement events constitute the critical measurement episode; in this case the precision should be interpreted as the uncertainty requirement of the average. The precision numbers in the tables are changed to uncertainty numbers. The relation to precision and uncertainty (σ) is given in formula (1).

$$\sigma^2 = \sigma_P^2 + \sigma_M^2 + \sigma_S^2 + \sigma_{other}^2 \qquad (1)$$

Uncertainty (σ) contains the following components: σ_P (Precision), σ_M (Matching), σ_S (Sample variation) and σ_{other} (inaccuracy and other effects). We assume normal distributions where each factor is independent and only random variations occur. [5]

Table MET3 Lithography Metrology (Wafer) Technology Requirements

Table MET4a Lithography Metrology (Mask) Technology Requirements: Optical

Table MET4b Lithography Metrology (Mask) Technology Requirements: EUV

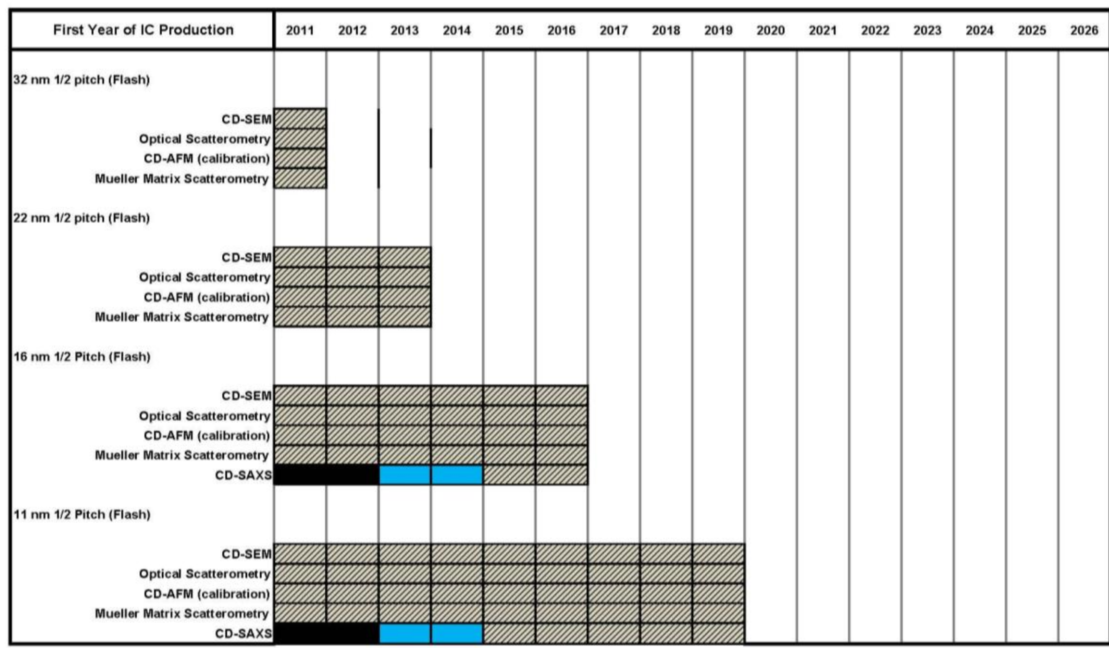


Figure MET1 Lithography Metrology Potential Solutions

5. FRONT END PROCESSES METROLOGY

The industry continues to find means of extending CMOS. The recent announcement that FinFET transistors will be introduced into manufacturing for the 22 nm ½ pitch indicates that future CMOS will be both planar and non-planar. Ultra-thin body SOI is expected to extend planar CMOS, and the scaling of SOI thickness may slow over the next ten years. Since first generation high κ and metal gate is in manufacturing, research and development efforts are aimed at increasing κ. Mobility enhancement through local stress remains a key means of scaling transistors. New channel materials will further enhance mobility. FinFET transistors are expected to use high κ and metal gate while increase in mobility will be achieved using different technology than that used for planar CMOS. The metrology community continues research and development to fill these measurement needs. It is important to note that characterization and metrology must be tailored to the specific process used to fabricate the transistor. IC manufacturers continue to use a variety of different designs, and transistor design is a differentiator for IC manufacturers. Examples of these differences can be highlighted by PMOS process and design for previous technology generations. Although the dual stress liner approach is predominant, but the use of SiGe in the source and drain is also used in manufactured IC's. Transistor cross-sections also show a variety of spacer oxide dimensions and processes. In this section the specific metrology needs for starting materials, surface preparation, thermal/thin films, doping technology, and front-end plasma etch technologies are covered. Process integration issues such as variability, the need to control leakage current, and the reduction in threshold voltage and gate delay and their tolerances will interact with the reality of process control ranges for gate dielectric thickness, doping profiles, junctions, and doses to drive metrology needs. Modeling studies of manufacturing tolerances continue to be a critical tool for transistor metrology strategy. Metrology requirements for Front End Processes are shown in Table MET5, and the potential solutions are shown in Figure MET4.

Table MET5 Front End Processes Metrology Technology Requirements

The impact of shrinking dimension on FEP metrology is already at the point where research devices and materials exhibit materials properties associated with nano-science. For example the properties of nanowire like shapes such as a FIN in a FINFET are quantum confined in two dimensions.

5.1. STARTING MATERIALS

Many of the metrology challenges related to starting materials involve the emerging class of layered materials such as SOI and strained silicon on SOI. The trend toward thinner layers, along with multiple layer interfaces, poses a challenge to most material metrology techniques.

Areas of concern include the following:

- Bulk Ni and Cu measurement on p+, silicon on insulator (SOI), strained silicon (SSi), and strained silicon on insulator (SSOI) wafers
- Measurement of 10^9–10^{10} cm^{-3} Fe (and other bulk metals) in the top Si of thin SOI wafers
- Thickness and uniformity of very thin SOI layers (<20 nm)
- Defectivity of thin layers (e.g., threading dislocations, “HF defects”)
- Particle detection (<100 nm) on layered surfaces

Small particle detection continues to be of concern for the future. Note that due to metrology capability issues the silicon starting materials particle requirements below 65 nm size will not require sub-65 nm metrology but will model the critical number of sub-65 nm particles based upon the number of particles detected at 65 nm size. More information can be found in the Starting Materials section of the *Front End Processes chapter*.

Silicon-On-Insulator (SOI) is entering the mainstream of IC device applications, and this is expected to grow further along the Roadmap. Recent device work has motivated a prediction of an increase in SOI thickness at 22 nm ½ pitch from 7 nm of Si to ~ 10 nm. This is predicted to follow another decrease in thickness for several ½ pitch nodes. This prediction may not follow the FEP roadmap SOI timing. One unmet challenge is the measurement of SOI uniformity inside die-sized areas. Across-wafer uniformity must also be characterized. An expectation has been that the materials specifications for polished silicon substrates would be transferred to SOI specifications. However, the underlying insulator structure in SOI negatively affects many of the metrology capabilities used for polished silicon substrates. Thus, there is some difficulty to measure and control SOI material properties at the level desired. The metrology community has addressed this but some issues remain. For more details on these metrology challenges see the FEP chapter on Starting Materials.

5.2. SURFACE PREPARATION

In situ sensors for particles, chemical composition, and possibly for trace metallics are being introduced to some wet chemical cleaning tools. Particle detection is covered in the *Yield Enhancement chapter.* Particle/defect and metallic/organic contamination analyses are covered in the Materials Characterization Section of the *Metrology* chapter. The role of impurities in high-κ gate dielectrics, and therefore their measurement requirements, is a future research topic. For the present the required impurity levels are projected to be the same as for silicon oxynitride gate dielectrics, but the measurement of those impurities is not clear.

5.3. THERMAL/THIN FILMS

Next generation high κ / metal gate technology may use nano-crystalline Hf based oxides. As these alternative oxides are being developed, new metrology challenges are emerging. The high κ gate stack contains several significant challenges that require further research and development. The Metrology roadmap previously discussed the challenges associated with measurement of nitrogen concentration in high-κ dielectrics. If nano-crystalline films are used, film crystal structure must be characterized to determine phase and texture. The composition of work function adjusting films must also be characterized. The films used to adjust the gate work function are very thin and nanoscale roughness may prove to be of the same dimensions as film thickness making it impossible to use some traditional measurement methods. Materials characterization of annealed gate stacks challenges all methods including ultra-high resolution TEM. In addition, new DRAM structures that use mixed high-κ dielectrics, and even ultra-thin layers of stacked high-κ dielectrics, will challenge metrology development.

Metrology research and development is required for advancement of new channel materials including germanium and III-Vs. Measurement needs are driven by the challenges associated with producing defect free crystal structures due to lattice mismatch with the silicon substrate. Measurement needs include observation and quantification of defect states in the band gap and dislocation densities. Many measurements require blanket films. At this time, correlation of measurements of blanket films with channel layers in transistors will require use of cross-sections which may not be representative of the total transistor structure.

5.4. STRAINED SI PROCESSES

Carrier mobility enhancement through process or structure induced local stress is a critical means of improving drive current and thus transistor performance. Typically, NMOS transistors are given tensile stress by applying Si_3N_4 stress liner film over the gate electrode. One of several different processes is used for PMOS transistors. In the replacement source-drain process, PMOS transistor channels are given compressive stress by the replacement of the silicon in the source and drain with selectively grown SiGe. The second means is through a compressive Si_3N_4 stress liner. Shallow trench isolation (STI) is another source of compressive stress in the channel. Here, the pattern layout of active area, gate electrode, and contact hole must be carefully designed and the processes should be tightly controlled. A combination of techniques and selection of Si crystal orientation in the channel have also been proposed. New processes in the development phase require stress characterization and metrology. These include a Si:C (heavily carbon-doped silicon) replacement source-drain process which is under consideration for NMOS. SiC would induce tensile stress in the NMOS channel region. As changing the materials of gate electrodes and by introducing so-called Gate Last process, sources of stress has been increasing. Thus necessity of local stress metrology technique is highlighted. It is known that Through Silicon Via (TSV) is another source of stress. In order to eliminate negative effect on transistors near TSVs, a metric of Keep Out Zone (KOZ) is introduced. Another explanation of stress measurement is shown in the sub-chapter of 3D interconnect metrology.

In order to accelerate design of the pattern layout and process conditions, a non-destructive direct measurement of the stress in the nano-sized area is desired. The importance of Finite Element Simulations of stress and resulting electrical properties has already been shown to be a key aspect of process development and metrology. Accurate stress metrology can help calibrate these simulations. As new processes are introduced with new technology generations, the challenge renews itself. Further complicating the challenge is the timing of the potential transition to alternate channels and the introduction of FINFETS or Trigate structure. Line items for local stress/strain measurements for both of off-line and in-line metrology were introduced to the metrology technology requirements Table MET5. It is expected that test pad would be used for in-line stress/strain measurement and its size is estimated at around 100 µm × 100 µm. This test pad size should be reduced as same as another metrology test pad such for film thickness measurement or OCD measurement.

Review of Stress Measurement Methods is shown in Figure MET2. This review shows a clear contrast in spatial localization capability between off-line methods such as NanoBeam Diffraction (NBD) and potential in-line methods from the stand points of off-line destructive metrology and in-line non-destructive metrology. In the case of Raman spectroscopy, area of measurement depends not only on microscopic spatial resolution but also wavelength of illumination light. This is due to the penetration depth of the light.

Area of Interest	Measurement Method	Sensitivity Stress	Sensitivity Strain	Measurement Area	Sample Thickness	
Transistor Level	- EBSD (SEM)	?	?	<10nm?		Non-Destructive
	- CBED (TEM)	20 MPa	0.02%	10-20nm	<100nm	Destructive
	- NBD (TEM)	100 MPa	0.1%	~10nm	<300nm	Destructive
	- TERS (Raman)	50 MPa	0.05%	<50nm		Destructive Non-Destructive
Micro-Area Level	- Confocal Raman	20 MPa	0.02%	~150nm		Non-Destructive
	- XRD	10 MPa	0.01%	100um		
	- Photo reflectance Spectroscopy	<20MPa	<0.02%	1um		
Die	- Die level flatness - Laser Interferometry - Coherent Gradient Sensing					Non-Destructive
Wafer	- Laser Interferometry - Coherent Gradient Sensing					Non-Destructive

* Stress – Strain relation : need to be clarified

TERS (Tip Enhanced Raman Scattering)
CBED (Convergent Beam Electron Diffraction)
NBD (Nano Beam Electron Diffraction)
XRD (X-ray Diffraction)

Figure MET2 Review of Stress/Strain Measurement Methods

5.5. FERAM

Although the thickness of the dielectric films are 100 to 200 nm, optical models for inline film thickness measurement of the metal oxides must be developed when a new materials set is used. The main metrology need is for fatigue testing of the capacitor structures at 10^{16} read write cycles and above.

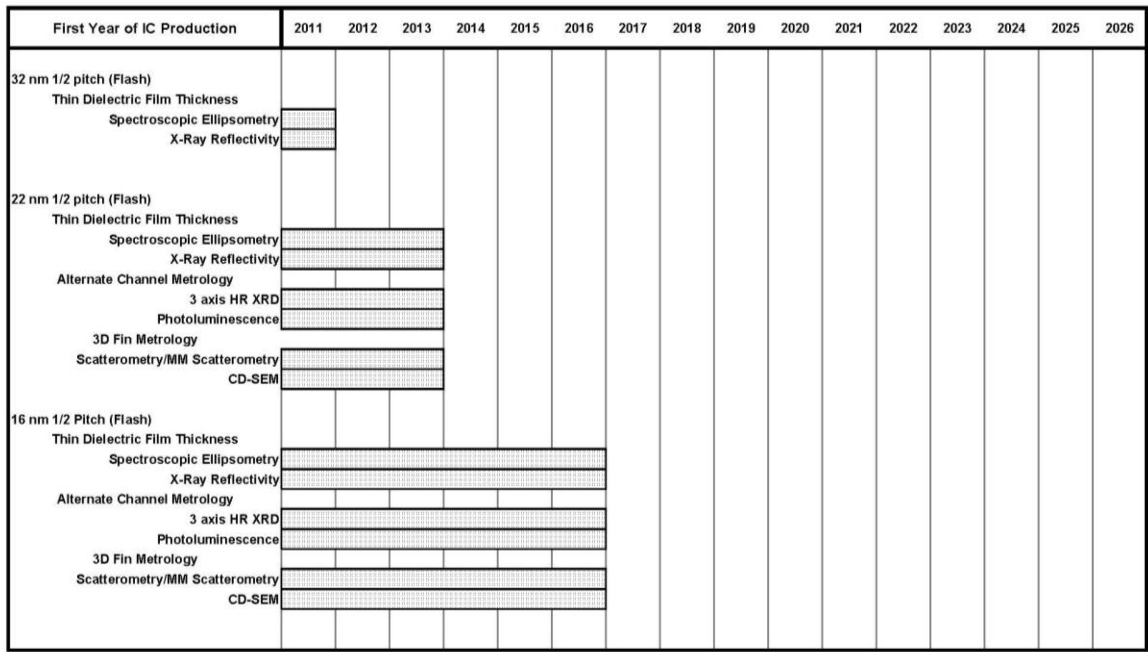
Cross-sections of memory devices illustrate the challenges associated with fabrication and process control for complex 3D memory structures created in a sequence of at least two patterning levels (pattern over pattern). Many measurement needs are not covered by simplified test structures. The impact of overlay errors is illustrated in Figure MET3. Cross-sectional metrology needs such as improved dimensional precision are a key requirement for memory and other 3D structures.

Figure MET3 3D Metrology Requirements

5.6. Doping Technology

Improved inline process measurements to control active dopant implants is required beyond 32 nm. Presently, 4-point probe measurement is used for high dose implant and photomodulated optical reflectance (PMOR) is used for low-dose implant process control. PMOR has been shown capable of measuring active dopant profiles. Advances in PMOR are needed to extend it to thin SOI. A new technique that provides direct *in situ* measurement of dose, dopant profile, and dose uniformity would allow real-time control. New methods for control of B, P, and As implants are also needed, and several inline systems based on x-ray/electron interactions optimized for B, P, and As dose measurement have recently been introduced. Offline secondary ion mass spectrometry has been shown to provide the needed precision for current technology generations including ultra-shallow junctions. The range of applicability and capability of new, non-destructive measurement methods such as carrier illumination (an optical technology) are under evaluation. Two- and preferably three-dimensional profiling of active dopant concentrations is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology. Nanoscale scanning spreading resistance (SSRM) measurements done in high vacuum have proven capable of achieving the necessary spatial resolution for dopant concentration gradients. Recent results indicate that HV-SSRM is capable of measuring between 1 and 1.5 nm/decade in carrier concentration with a precision of between 3 to 5%.

The measurement of dopant profiles in 2D/3D structures, such as FINFETs, is a challenge. Indirect methods such as fin resistivity in test structures may detect process changes, but the direct determination of the dopant profile and its conformality is difficult.



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

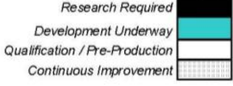


Figure MET4 FEP Metrology Potential Solutions

6. 3D INTERCONNECT METROLOGY

3D Interconnect process technology is covered in both the Assembly and Packaging as well as the Interconnect Roadmaps. The main challenges for 3D metrology involve measuring high aspect ratio through-silicon vias (TSV), and the opaque nature of materials (silicon, copper) that limit optical microscopy techniques. These challenges are characterized by two different tool sets; in-line metrology and off-line metrology using destructive analysis.

Development of manufacturable 3D processes is also dependent upon a broad range of existing semiconductor metrologies including but not limited to; thin film metrology, packaging metrologies and electrical test. These metrologies are not addressed in this section of the ITRS.

Table MET6 ITRS 3D Interconnect TSV Roadmap

GLOBAL LEVEL, WTW, DTW, or DTD 3D stacking	2009-2012	2012-2015
Minimum TSV diameter	4-8 µm	2-4 µm
Minimum TSV pitch	8-16 µm	4-8 µm
Minimum TSV depth	20-50 µm	20-50 µm
Maximum TSV aspect ratio	5:1-10:1	10:1-20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch (thermocompression)	10 µm	5 µm
Minimum contact pitch (solder or SLID)	20 µm	10 µm
Number of tiers	2-3	2-4
INTERMEDIATE LEVEL, WTW 3D stacking	**2009-2012**	**2012-2015**
Minimum TSV diameter	1-2 µm	0.8-1.5 µm
Minimum TSV pitch	2-4 µm	1.6-3 µm
Minimum TSV depth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1-10:1	10:1-20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch	2-3 µm	2-3 µm
Number of tiers	2-3	8-16 (DRAM)

6.1. Bonding Overlay

Validation of the performance of process equipment for bonding wafers for 3D interconnects will require the use of infrared (IR) microscopy to measure alignment fiducials at the interface of the bonded wafer pairs (BWP), comparing overlay error to overlay tolerance, then determining if overlay accuracy is sufficient for electrically yielding interconnects. Silicon is transparent to IR radiation, which is able to penetrate through full thickness (775 microns thick for 300mm diameter wafers) silicon wafers, enabling the measurement of overlay.

Currently, there are a number of IR microscope tools capable of supporting in-line overlay metrology requirements for bonded wafer pairs in high volume manufacturing (HVM). They use either broadband IR (typically from a halogen lamp), or a specific IR laser generated wavelength (typically 1310 nm). An IR metrology tool for this purpose and has demonstrated repeatability of overlay measurements on bonded wafer pairs with 1 sigma repeatability of less than 0.1 µm. The spatial resolution of this system based upon the Rayleigh criterion is ~ 0.5 µm. In the case where the carrier substrate is transparent to visible light, the use of metrology equipment with a Top and Bottom microscope configuration can also be an alternative solution. This configuration can also demonstrate repeatability 1 sigma of less than 0.1microns.

Using in-line overlay metrology is necessary to identify poorly aligned wafer pairs that are unlikely to provide electrically yielding interconnects. As a result, those costs and time associated with subsequent wafer processing are avoided, and the feed-back loop for bonding process control is closed. IR microscope resolution at 0.5 micron matches the interconnect roadmap for overlay accuracy 2009 – 2012. Improved overlay accuracy as specified in the roadmap requires an improvement in overlay resolution for 2012 and beyond.

Overlay performance is an inherently 2D parameter. Circular via features are bonded to circular bond pads, in patterns that span the full size of the wafer pair. Most statements of overlay performance focus on performance in a single axis. Definitions of overlay that are consistent with the multi-dimensional nature of the actual requirement and test methods that account for overlay performance throughout the entire wafer area should be defined in ITRS 2011.

6.2. Bonded Interface Void Detection

Good bonding at the interface of a bonded wafer pair is critical to ensure that the wafer pair does not separate during subsequent operations like wafer thinning and wafer bevel edge trim. Scanning acoustic microscopy (SAM) has proven useful to detect and characterize bond voids at the interface of a BWP. Using transducers (typically 110 MHz) to create ultrasound, and a couplant liquid to transmit ultrasound to the BWP surface (typically DI water), SAM can survey the interface of a bonded wafer pair and detect voids as reflections of ultrasonic energy. SAM resolution is improved by

using higher frequency ultrasound and thinning wafers to decrease ultrasound attenuation, but thinning wafers to achieve improved SAM resolution is not a manufacturable solution for metrology in HVM. The throughput of this method must also be improved for volume production.

Currently, there are a number of SAM tools capable of supporting in-line void metrology requirements for bonded wafer pairs in high volume manufacturing. Dry-in, dry-out SAM systems that use a Nitrogen stream to remove couplant liquid from the external surfaces of a bonded wafer pair are available. There is some concern for added defectivity as a result of the couplant liquid used (particles, metallics), but subsequent thinning operations and the cleaning steps that follow are expected to be sufficient for reducing SAM-induced defects. Another concern is lack of heremeticity at the interface of the bonded wafer pair that can allow couplant liquid incursion into the interface via capillary action. The use of a liquid spray instead of complete immersion could be an attractive alternative.

Using in-line void metrology is necessary to identify wafer pairs that have the potential to separate during subsequent wafer thinning and edge bevel trimming operations. SAM resolution for BWP voids approaches 60 microns (using a 110MHz transducer). Although there is no bond void requirement specified in the ITRS, it is recommended to be included in the 2011 revision.

6.3. Bonded Interface Defect Identification

Currently, there are no metrology tools capable of supporting in-line bonded wafer pair defect identification with defect mapping in a Cartesian coordinate system for subsequent defect review. Although there is no BWP defect identification requirement specified in the ITRS, it is recommended that it be included in the 2011 revision.

6.4. Bonded Interface Defect Review

Bonding wafers for 3D interconnects will require the use of infrared (IR) microscopy to locate and review defects at the interface of a bonded wafer pair. These defects are present on individual wafers prior to bonding (particles, CMP damage) or generated during the bonding process (voids, adhesive anomalies, dendritic structures) . BWP defect review tools will need to be able to merge individual wafer defect maps into a combined BWP map, and will require the ability to add any new defects randomly observed during defect review.

Currently, there are defect review tools using an IR microscope capable of supporting defect review requirements for bonded wafer pairs in high volume manufacturing. An IR microscope is not useful as a defect identification tool as outlined in section 2.3. The field of view of the microscope is relatively small, and 100% inspection of the entire wafer is not feasible. However, defects can be manually identified at the interface of the BWP and added to its defect map. Although there is no BWP defect review requirement specified in the ITRS, it is recommended that it be included in the 2011 revision.

6.5. Edge Bevel Defects

Edge bevel inspection is required to identify defects in a bonded wafer pair that can lead to subsequent wafer breakage. Edge bevel defects can be problematic at bonding. Edge bevel chips can initiate cleave lines for silicon wafer breakage when the forces associated with bonding or thinning wafer pairs are applied. The control of the notch alignment of bonded wafer pairs with an accuracy of less than 50 microns is also needed. Wafer edge bevel trim operations that precede bonded wafer pair thinning can be another source of edge bevel defects.

Currently, there are a number of edge bevel inspection tools capable of supporting in-line metrology requirements for bonded wafer pairs in high volume manufacturing. Although there is no edge bevel defect requirement specified in the ITRS, it is recommended that it be included in the 2011 revision.

6.6. Bond Strength Uniformity

Currently, there are no in-line tools to assess bonded wafer pair strength uniformity. Micro-chevron testing for BWP strength uniformity uses a wafer with an etched pattern (micro-chevron), bonded to a blanket film wafer that is subsequently speciated into individual die and tested for adhesion strength using a pull-tester. Mapping bonding strength results for multiple die on a BWP allows calculations for within-wafer pair non-uniformity, and indicates adjustments to the wafer bonding hardware are required when strength uniformity results drift outside of established control limits. Micro-chevron testing is more sensitive and repeatable than other bond strength tests like 4-point bend.

Although there is no BWP strength uniformity requirement specified in the ITRS, it is recommended that it be included in the 2011 revision by specifying micro-chevron testing as described in SEMI® standard MS-5.

6.7. BONDED WAFER PAIR THICKNESS

Total thickness and intra-wafer total thickness variation (TTV) of the BWP is crucial for the bonding and grinding operation. Currently, there are a number of metrology tools capable to support in-line measurement. Traditional capacity method technique has limitation in the case of non-conductive substrate. The white light or IR chromatic as well as interferometry technique can provide very good alternative for total thickness measurement when implemented in a top and bottom dual mode configuration.

The measurement of individual layers consisted of the BWP will generally require the use an IR light source to pass through the Silicon layers. The drawback of the IR interfometer technique is lack of resolution for thin layers. With improvement in detection treatment algorithm, thin layers such as the adhesive layer itself could be measured.

6.8. TSV ETCH DEPTH

Through-silicon vias are etched at a very high aspect ratio (HAR) of via diameter to etch depth, approaching 10:1 - 20:1. These HAR features challenge and limit the use of optical metrology techniques for measuring smaller diameter TSVs.

Currently, there are a number of TSV etch depth metrology tools capable of supporting in-line metrology requirements in high volume manufacturing. Depending on the principle of the techniques involved and its spot size, the measurement can be done on individual TSV, on an average number of TSVs or will require a specific periodic array of TSVs.

White light interferometry and backside infrared interferometry can be used for measuring etch depth of individual TSVs for 5 micron and larger diameter TSVs with less than 10:1 aspect ratio. For white light interferometer and smaller diameter, improvement in sensor configuration is needed to get paralleled collimated light to able to be reflected down to the bottom TSV. Backside infrared interferometry has been demonstrated as capable for TSV etch depth metrology for sub-micron features, and is not limited by aspect ratio.

The model based infrared reflectometry on an array of TSVs could be another alternative for depth measurement of diameter below 5microns at the condition the density of via is high enough to get diffracted signal. This technique is not a direct technique and will require cross-section analysis for calibration.

Although there is no TSV etch depth metrology requirement specified in the ITRS, it is recommended that it be included in the 2011 revision.

6.9. TSV ETCH PROFILE

Currently there are no in-line TSV etch profile metrology tools suitable for use in high volume manufacturing. Cross-section SEM analysis can be utilized for process development, but it is a destructive technique. Although there is no TSV etch profile metrology requirement specified in the ITRS, it is recommended that it be included in the 2011 revision.

6.10. TSV LINER, BARRIER, SEED THICKNESS

Deposition of liner, barrier and seed films is challenged by the high aspect ratio of the TSV and directional film deposition processes. Continuous, pin-hole free films in the TSV are required to electrically isolate, prevent copper migration and encourage good copper fill in the subsequent copper plating process.

Currently there are no in-line tools suitable for TSV liner, barrier and seed thickness metrology for use in high volume manufacturing. Cross-section SEM and TEM analysis can be utilized for process development, but are destructive techniques. Electrical test structures can be utilized for measuring leakage and electro-migration, but the information they provide is obtained after many subsequent operations following liner, barrier and seed deposition.

Although there are no TSV liner, barrier and seed thickness metrology requirements specified in the ITRS, it is recommended that they be included in the 2011 revision.

6.11. TSV VOIDS

Micro-voiding in the TSV or in the interconnect bond region could lead to electrical or reliability failures. Using standard cross-sectioning or FIB/SEM techniques it is possible to destructively evaluate the condition of a selected bonded vias. Non-destructive methods to identify these defects would provide significant benefits for both process development and failure analysis.

TSV void metrology is challenged by the opaque nature of copper; optical metrology techniques for void detection are not available. Acoustic wave techniques are also investigated through the change in total volume of the copper lines. The capability to scan the whole TSV depth as well as the sensitivity to micro-void has to be demonstrated. Copper plating is

challenged by the high aspect ratio of the TSV; any tendency towards conformal plating must be carefully controlled by plating bath additives to ensure bottom-up filling.

X-ray and x-ray tomography techniques have proven useful to reveal voids within copper-filled TSVs, but are slow and require destructive sample preparation. X-ray tools cannot be considered as in-line TSV void metrology for high volume manufacturing, but are useful for feedback on TSV plating process development.

Although there is no TSV void metrology requirement specified in the ITRS, it is recommended that it be included in the 2011 revision.

6.12. SHAPE AND STRESS

The shape of the BWP is usually controlled through Bow and warp measurements over the process flow. This is critical for process monitoring but also for all aspects related to handling of thin wafers in a manufacturing context. Currently there are a large number of metrology tools capable to support these in-line measurements. Various techniques such as laser deflection, capacity, chromatic and interferometer techniques, coherent gradient sensing (CGS) are able to give the shape of the BWP. As it stands, the results strongly depend on the way the wafer is hold and at some point can be impacted by gravity effect. Coherence between metrology semiconductors suppliers need to be improved through SEMI standard recommendation. This will allow comparable results between techniques.

The introduction of large scale TSV in CMOS environment is also raising the question of stress induced by the TSV themselves. Raman spectroscopy can measure stress distribution in the Silicon around the TSVs using small spot but the technique needs to move to longer wavelength to get information from deep silicon. Off-line analysis such as XRD and ESBD techniques are also implemented alternatives to get the strain measurement.

6.13. 3D METROLOGY FOR COPPER NAIL AND PILLARS

For future 3D interconnect technologies, such as stacking circuit blocks and 3D integrated circuit, there is a need to control the height, diameter and coplanarity of the Copper pillars that will connect the top and bottom of the stacked dices. This request pretty much equivalent to Bumps measurements in backend manufacturing plants becomes now also critical at the wafer level for IC manufacturing.

There are a number of metrology tools capable to measure those parameters at a production scale. Techniques such as laser triangulation or confocal interferometry are very well adapted. Nevertheless there is clearly a lack of reference standard available to address deficiencies for 3D metrology.

7. INTERCONNECT METROLOGY

New processes, novel structures and aggressive dimensional scaling continue to drive metrology research and development for interconnect technology. Increasingly porous low κ dielectric materials are moving into manufacturing, and 3D Interconnect is being used in a great variety of implementations. Copper contact structures were announced at key technical symposia. All areas of metrology including materials characterization, in-line measurements, and advanced equipment and process control are used for interconnect research, development, and manufacturing. As copper / low k interconnects continue to scale in both reduced dimension and increased porosity, the metrology challenges become more difficult. In particular barrier conformality of 2 nm films, the presence of 3 nm sized voids in copper lines, the size and crystallographic orientation of nm sized copper grains, the size and connectivity of nm sized pores in dielectrics and the characterization of etch residue, etch damage and barrier penetration into porous low k films all become more challenging. As dimensions approach the few nm scale, interfacial effects can drive very large perturbations in dielectric constant, grain boundary scattering, thermal conductivity and barrier effectiveness. The need to integrate multi-layer stacks of low k dielectrics with ever decreasing mechanical and chemical stability requires techniques which can characterize the stress and chemical states of these amorphous materials. In addition to scaled copper / low k interconnects, new interconnect solutions such as optical, carbon and spin based interconnects have their own metrology challenges. While the characterization of the optical properties of blanket dielectric films is routine to the semiconductor industry, the determination of optical loss due to sidewall roughness and measurements of the electro-optic effect of optical modulator materials is far from routine and usually requires complex, integrated test structures. While process has been made on determining the chirality of carbon nanotubes, there are challenges to determining the bandgaps of narrow graphene ribbons and scattering lengths for spin polarized transport in more speculative interconnect options.

Interconnect needs for metrology, as noted above, include continuing evolutionary advances in existing metrology techniques, as well as the increasing need for novel metrology approaches for more radical interconnect structures. The following sections will describe some of the needs and status of existing metrology techniques for copper and low-k

Interconnects. The preceding section focused on the needed advances for future directions in 3D interconnect. Refer to the *Interconnect chapter*.

7.1. CU-LOW κ METALLIZATION ISSUES AND METROLOGY NEEDS

7.1.1 CU METALLIZATION ISSUES

Copper metallization has been used in high volume manufacturing for over six generations. With each shrink, the challenges of filling trenches and vias must be faced again. Among the most important of these are characterizing barrier conformality, detecting nm sized voids, determining the size and orientation of Cu grains and the need for precise control of electrochemical deposition baths. Voids in metal lines and vias that occur during processing have been identified as significant yield loss initiators. Voiding problems can show up after deposition/CMP/anneal, or from agglomeration of micro-voids due to electro or stress migration. Another significant problem relating to voids is a need to be able to identify relatively small, isolated voids in large fields of patterned Cu conductors. These isolated voids often do not show up as yield loss, but can be an incipient cause of later reliability failures. These voids may be on the surface of the conductors, but are often buried within the conductor pattern or in vias. Additional issues with Cu metallization arise from the use of thin barriers to isolate the Cu from underlying dielectrics. These thin barriers raise significant needs for measurement capabilities of ultra-thin layers, interface properties, and defects and materials structure on sidewalls in very narrow channels. These needs require the ability to not only establish physical properties and structure of these layers with thicknesses <2 nm but also identify and characterize defects in the films. An additional problem area is the characterization of the interfaces between the Cu electroplated layer, the Cu seed, the barrier layer and the dielectric. As the Cu conductors become smaller, both grain boundary and sidewall interface scattering will cause significant increases in resistivity of very narrow lines.

7.1.2 CU METALLIZATION METROLOGY

Copper electroplating systems need quantitative determination of the additives, byproducts, and inorganic contents in the bath to maintain the desired properties in the electroplated copper film. Process monitoring requires *in situ* measurements of additives, byproducts, and inorganic content that result from bath aging. A mass spectrometry based method to real-time sample bath contents provides a new potential solution. Cyclic voltammetric stripping (CVS) is widely used to measure the combined effect of the additives and byproducts on the plating quality. Liquid Chromatography can be used to quantitatively measure individual components or compounds that are electrochemically inactive and volumetric analysis using titration methods can be used for the monitoring of inorganics.

Barrier layer metrology needs include measurement of thickness, spatial uniformity, defects, and adhesion. Inline measurement for 3D structures continues to be a major gap. Measurement of materials on sidewall of low κ trenches is made even more difficult by the roughness along the sidewall. There is some concern about the application of statistical process control to very thin barrier layers. Barrier layers for future technology will be <2 nm thick. Presently, a number of measurement methods are capable of measuring a barrier layer under seed copper when the films are horizontal. These methods include acoustic methods, X-ray reflectivity, and X-ray fluorescence. Some of these methods can be used on patterned wafers. EXAFS measurements have also been applied to the characterization the properties of self-forming barriers in integrated structures. Inline measurement of crystallographic phase and crystallographic texture (grain orientation) of copper/barrier films is now possible using X-ray diffraction and electron back-scatter diffraction based methods. This technology is under evaluation for process monitoring, and the connection to electrical properties and process yield is being investigated.

Detection of voids in copper lines is most useful after the CMP and anneal processes. A metric for copper void content has been proposed in the Interconnect Roadmap and in line metrology for copper voids is the subject of much development. However, these efforts are focusing on the detection of voids only and not on the statistical sampling needed for process control. Many of the methods are based on detection of changes in the total volume of the copper lines. The typical across-chip variation in the thickness of copper lines will mask the amount of voiding that these methods can observe. Interconnect structures, which involve many layers of widely varying thickness made from a variety of material types, pose the most severe challenge to rapid, and spatially resolved multi-layer thickness measurements.

Some measurements remain elusive. For example, measurement of barrier and seed copper film thickness on sidewalls is not yet possible. Recently crystallographic texture measurements on sidewalls have been reported. Adhesion strength measurements are still done using destructive methods. End point detection for etch must be developed for new etch stop materials for porous low κ. Other areas of metrological concern with the new materials and architectures include in-film

moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), and line resistivity (versus bulk resistivity). In addition, calibration techniques and standards need to be developed in parallel with metrology.

Development of interconnect tools, processes, and pilot line fabrication all require detailed characterization of patterned and unpatterned films. Currently, many of the inline measurements for interconnect structures are made on simplified structures or monitor wafers and are often destructive. Small feature sizes including ultra-thin barrier layers will continue to stretch current capabilities. Interconnect metrology development will continue to be challenged by the need to provide physical measurements that correlate to electrical performance, yield, and reliability. More efficient and cost-effective manufacturing metrology requires measurement on patterned wafers. Metrology requirements for Interconnect are shown in Table MET7 and the potential solutions are shown in Figure MET5 below. The new measurement requirements for void detection in copper lines and killer pores in low κ appear to be difficult or impossible to meet. The need is to have a rapid, inline observation of very small number of voids/larger pores. The main challenge is the requirement that the information be a statistically significant determination at the percentage specified in Table MET7.

Table MET7 Interconnect Metrology Technology Requirements

7.2. LOW κ DIELECTRICS ISSUES AND METROLOGY NEEDS

7.2.1 LOW κ DIELECTRIC ISSUES

The move from SiO_2 to porous low κ dielectrics in interconnect structures has proven to be a more difficult challenge to the semiconductor industry than the move from Al metallization to Cu. A significant part of the difficulties has come from the fact that low κ materials available thus far have significantly different physical and mechanical properties than the prior SiO_2. Among the primary differences are significantly different mechanical properties, chemistry and the presence of pores in the material. The lower mechanical strength has resulted in a new set of issues stemming from problems resulting from materials and processes used in back end manufacturing showing up as problems at assembly and packaging. A significant part of the problem is that there is no convenient and competent metrology tools and methodology to qualify materials at the back end process stage for assembly and packaging viability. A second major issue has been identified with characterization of porous materials. At the present time there are no metrology techniques and methodologies to identify anomalously large or significantly connected pores (so called “killer pores”) in otherwise smaller pored materials. There are also no available metrology techniques to characterize the materials on the sidewalls of low κ patterns for physical properties, chemical structure, and electrical performance. This capability needs to be able to identify and quantify very thin layers on these sidewalls related to physical layers and damage due to processes such as pore sealing and plasma etch damage. These features need to be quantifiable both on continuous sidewall surfaces and into pores on porous materials. The two issues noted above, along with the standard measurements associated with dielectrics; need to be addressed for not only today’s dielectrics, but also for those that will be used in the few nanometer generations of the not too distant future.

7.2.2 LOW-κ METROLOGY

Inline metrology for non-porous low κ processes is accomplished using measurements of film thickness and post CMP flatness. *In situ* sensors are widely used to control CMP. Metrology continues to be a critical part of research and development of porous low κ materials. The need for transition of some of the measurements used during process development into volume manufacturing is a topic of debate. Examples include pore size distribution measurement. Pore size distribution has been characterized off-line by small angle neutron scattering, positron annihilation, a combination of gas absorption and ellipsometry (ellipsometric porosimetry), and small angle X-ray scattering (SAXS). SAXS and ellipsometric porosimetry can be used next to (at-line) a manufacturing line. The need for moving these methods into the fab is under evaluation. Detection of large, “killer,” pores in patterned low κ has been highlighted as a critical need for manufacturing metrology by the Interconnect Roadmap.

High-frequency measurement of low κ materials and test structures has been developed up to 40 GHz to determine both frequency dependent dielectric constants and loses. This meets the needs for clock rates of up to about 5 GHz. In general, low-κ materials seem to have nearly constant dielectric functions over the frequency range of interest (from 1 GHz to 10 GHz).

Thinning of porous low κ during chemical mechanical polishing technology must be controlled, and available flatness metrology further developed for patterned porous low-κ wafers. Stylus profilers and scanned probe (atomic force) microscopes can provide local and global flatness information, but the throughput of these methods must be improved. Standards organizations have developed (and continue to develop) flatness tests that provide the information required for statistical process control that is useful for lithographic processing.

Interconnect specific CD measurement procedures must be further developed for control of etch processes. Key gaps include the ability to validate post etch clean effectiveness, sidewall damage layer and properties. Angle resolved photoelectron spectroscopy has shown some success at characterizing nm thick residue and chemical modifications on sidewalls. Rapid 3D imaging of trench and contact/via structures must provide profile shape including sidewall angle and bottom CD. This is beyond the capabilities of current inline CD-SEMs. Etch bias determination is difficult due to the lack of adequate precision for resist CD measurements. One potential solution is scatterometry, which provides information that is averaged over many lines with good precision for M1 levels, but this precision may degrade for higher metal levels. Furthermore, scatterometry must be extended to contact and via structures. Other techniques with potential include 3D AFM and He ion microscopy. Electrical test structures continue to be an important means of evaluating the RC properties of patterned low-κ films.

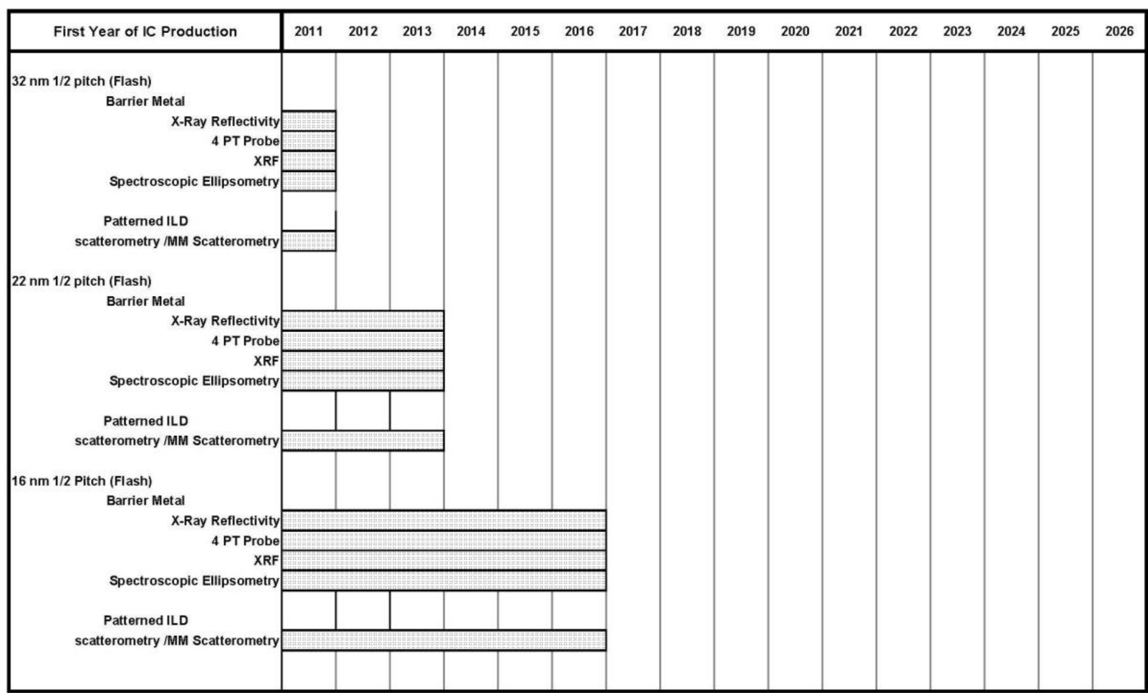


Figure MET5 Interconnect Metrology Potential Solutions

8. MATERIALS AND CONTAMINATION CHARACTERIZATION

The rapid introduction of new materials, reduced feature size, new device structures, and low-temperature processing continues to challenge materials characterization and contamination analysis required for process development and quality control. Correlation of appropriate offline characterization methods, with each other, and with inline physical and electrical methods, is often necessary to allow accurate measurement of metrics critical to manufactured device performance and reliability. Characterization accuracy requirements continue towards tighter error tolerances for information such as layer thickness or elemental concentration. Characterization methods must continue to be developed toward whole wafer measurement capability and clean room compatibility.

The declining thickness of films, moving into the sub-nanometer range, creates additional difficulties to currently available optical and opto-acoustic technologies. Shorter wavelengths of light even into the X-ray range are currently investigated to overcome the challenge of inline film thickness and composition detection. Complimentary techniques are

often required for a complete understanding of process control, for example X-ray reflectometry can be used to determine film thickness and density while UV ellipsometry can determine thickness, optical index, and band-gap.

Often, offline methods provide information that inline methods cannot. For example, transmission electron microscopy (TEM) and scanning TEM (STEM) can provide the highest spatial resolution or cross-sectional characterization of ultra-thin films and interfacial layers. STEM systems equipped with X-ray detection and electron energy loss spectroscopy (EELS) have provided new information about interface chemical bonding. High-performance secondary ion mass spectroscopy (SIMS), and its variant time-of-flight (TOF) SIMS, provide contamination analysis of surfaces and thin film stacks. Grazing incidence X-ray reflectivity (XRR) provides measurement of film thickness and density, while grazing incidence X-ray diffraction provides information about the crystalline texture of thin films. The importance of using diffuse scattering in addition to specular scattering during XRR seems to be critical to building interfacial models from XRR that can be compared to interfacial models from other methods such as TEM/STEM, SIMS, and ion backscattering. Field emission Auger electron spectroscopy (FE-AES) provides composition analysis of particulate contamination down to less than 20 nm in size. Offline characterization of physical properties such as void content and size in porous low-κ insulators, film adhesion, and mechanical properties, for example, is required for evaluation of new materials. Many of these tools are now available for full wafers up to 300 mm in diameter.

Continued development of TEM and STEM imaging capability is required. TEM/STEM methods require sample preparation methods that can result in metrology artifacts if care is not taken. Choice of detection angle for annular detectors employed in STEM instruments allows imaging contrast to vary from incoherent imaging sensitive to mass-thickness variations to coherent imaging sensitive to crystal orientation and strain. Several technologies are being applied to materials and process development for critical areas such as high and low κ. Electron energy loss spectroscopy (EELS) can achieve spatial resolution of atomic columns for oriented crystalline samples. With this greatly improved spatial resolution, EELS can be used to characterize interfacial regions such as that between high κ dielectrics and the silicon substrate. STEM with Annular Dark Field imaging and EELS are becoming routine in manufacturing support labs, however spatial resolution in regular practice is often limited by real device samples where amorphous and disordered interfaces increase probe interaction volumes beyond those afforded by channeling along atomic columns in perfect crystals. Further routine site-specific sample preparation conducted by focused ion beam generally produces samples in the 100 nm thickness range. For certain applications such as lithographic cross section metrology of photoresist and gate side wall angle measurements, this is sufficient. More challenging applications require a thickness of below 50 nm for optimal spatial resolution in imaging and analysis. Great advances have been made using *in situ* argon beam thinning of samples. Advances in image reconstruction software have also improved image resolution and thus interfacial imaging. Several improvements in TEM/STEM technology are now commercially available including lens aberration correction and monochromators for the electron beam. Recent breakthroughs in aberration corrected scanning TEM look very promising and reveal details such as single misplaced atoms in a junction. Further, via combined application with high-brightness electron sources, improved resolution may be achieved at reduced incident beam acceleration potentials allowing TEM measurements below the damage threshold energies that have plagued high resolution characterization of fragile materials including carbon nanotubes and graphene. All of these TEM/STEM tool improvements put added constraints on improved sample preparation; thinner samples and reduced surface-damage layers are required.

Though at present it's generally considered time-prohibitive, electron tomography, producing 3D models of device structures, may play an increasingly important role in metrology. Tomography has less stringent sample preparation conditions as surface damage regions may be removed from reconstructions and thicker samples are generally desired.

Advances over traditional energy dispersive spectrometers (EDS) and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. New X-ray detectors will allow resolution of slight chemical shifts in X-ray peaks providing chemical information such as local bonding environments. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks that cannot be resolved with current generation lithium-drifted-silicon EDS detectors. Although beta site systems have been tested, unfortunately, these have not become widely available. These detectors can also be implemented in micro XRF (X-ray fluorescence) systems, using either an electron beam or a micro focus X-ray beam as excitation source. XPS (X-ray photoelectron spectroscopy) is now widely used as a means to determine thickness and composition of thin (up to 50 nm) films.

While these and other offline characterization tools provide critical information for implementing the Roadmap, there are still many challenges. Characterization of high-κ gate stacks is difficult due to the length-scales for which electrical properties are determined. For example chemical intermixing by reactions forming intermetallics or alloys may be easily confused with physical roughness at an interface. Characterization techniques which probe the local atom-atom interactions including electron energy loss spectroscopy, X-ray absorption near edge structure spectroscopies are often

required. In addition, as device features continue to shrink and new non-planar MOS devices are developed, the applicability of characterizing planar structures as representative of device features becomes more questionable. Furthermore, ongoing scaling makes the analysis of contamination in high aspect ratio structures even more difficult.

The introduction of new materials will raise new challenges in contamination analysis, such as happened with copper metallization where the very real possibility of cross contamination has led to the need to measure bulk copper contamination down to the order of 10^{10} atoms/cm^{3} and surface copper contamination even in the edge exclusion and bevel regions, all because of the high diffusivity properties of this deleterious metal. Device shrinking is also tending to lower the thermal budgets allowed for processing so that the behavior of metal contamination and how to reduce its negative effects are changing the characterization needs. For example, low-temperature processing is changing which surface contamination elements, and at what levels, need to be controlled and therefore measured. A key example is the role of surface calcium on very thin gate oxide integrity, and the difficult challenge of measuring this surface element at the 10^{8} atoms/cm^{2} level. Traditional methods such as vapor phase decomposition followed by ICP-MS can have day-to-day limitations at this level. In addition, low-temperature processing is changing how metal contamination gettering is achieved, challenging the way to characterize material properties to ensure proper gettering.

Metallic contamination has long been known to be a key detrimental factor to device yield, causing degradation of electrical parameters like gate oxide breakdown voltage and background noise in Charge Coupled Devices (CCD) for instance. Historically, monitoring has been achieved in-line through the use of monitor wafers and a combination of Total Reflectance X-Ray Fluorescence (TXRF) and post anneal Surface Photo Voltage (SPV). Unfortunately, with the ever increasing sensitivity of new technologies to trace metal contaminants and the more stringent quality criteria imposed by certain applications, this type of control scheme often has limitations both in terms of sensitivity and detection capabilities. A technique like Automated Vapor Phase Decomposition / Ion Coupled Plasma Mass Spectrometry (VPD /ICP-MS) can be powerful in this context as ultimate detection limits can be reached (down to a few 106 at/cm2 for some species). Full or semi-local wafer measurement can be performed and tool automation enable insertion as a true monitoring tool in a production line. In addition bulk analysis can also be achieved through the use of adequate chemistries which in combination with DLTS (Deep level transient spectroscopy) can offer a full range analytical capability both in terms of identification and quantification.

8.1. Materials and Contamination in Strain-Based Devices

The accelerated use of strained silicon without SOI has resulted in new metrology and characterization requirements earlier than predicted. Gate oxide metrology becomes even more complex when strained Si channel structures are used as the starting material instead of bulk Si or SOI wafers. Strained Si is either grown on thick relaxed SiGe buffer layers on bulk Si or on compliant substrates consisting of thin SiGe layers on SOI. In both cases, the metrology of the starting material is crucial with a large number of parameters to be controlled: 1) thickness and Ge profile of the SiGe buffer, 2) thickness of the strained Si channel, 3) roughness of the Si/SiGe interface and the Si surface, 4) magnitude and local variation of stress in the Si channel, 5) threading dislocation density in the Si channel (high sensitivity of the measurement is needed, since the desirable dislocation density is very low (at $<10^{3}$-10^{4}cm^{-2})), 6) density of other defects, such as twins, dislocation pile-ups, or misfit dislocations, particularly at the SiGe/Si channel interface, and 7) distribution of dopants in channel and buffer (particularly after thermal annealing).

Several methods employing TEM/STEM have been developed to measure and map strain distributions in strained-channel devices. It has been noted that thinning of a TEM sample may allow relaxation of some of the strain, and finite element modeling has been useful in understanding how strain may be relaxed during sample thinning, however strain measurement by TEM/STEM has had many successes. Both threading and misfit dislocations can be measured by TEM, but the limited sample size area if often a problem for required statistical analysis of dislocation densities. Atomic force microscopy determines the surface roughness of the Si channel. Optical microscopy has been successful for etch pit density (EPD) measurements to determine the density of threading dislocations intercepting the wafer surface. Clear prescriptions for EPD are needed to select the etch depth. The meaning of lines and points in the EPD optical images need to be explained. X-ray topography is another technique offering promise for defect detection. The Ge and dopant profiles can easily be measured with SIMS. A high sputtering rate is needed for thick SiGe buffers, while high depth resolution (possibly with a low-energy floating ion gun) enables the analysis of the thin Si channel and of the channel/buffer interface. Optical carrier excitation using a red photodiode directed at the sputtering crater has been used to avoid SIMS charging artifacts; this is particularly important for strained Si over SOI and for undoped layers.

Unique properties associated with strained silicon are being addressed with a variety of metrology methods. Stress is the force required to create lattice strain which affects the electronic band structure to provide mobility enhancement of electrons or holes. Raman spectroscopy can measure stress, while TEM and XRD measure strain. Raman spectrometry

measures the energy of the Si-Si vibration in the Si channel which depends on changes in stress. However, the phonon deformation potential (describing the variation of the Si-Si phonon energy with stress) is not firmly established for thin Si channels. Such Raman measurements need to be performed using a UV laser to avoid penetration of the laser into the Si substrate. At 325 nm wavelength, the entire Raman signal stems from the thin Si channel, simplifying data analysis. For longer wavelengths, the Si-Si vibration in the SiGe buffer complicates the signal. The energy of the Si-Si vibration in SiGe depends on alloy composition and stress, which complicates the problem. Raman mapping yields the stress distribution across the wafer with a maximum resolution of about 0.5 μm, thus allowing prediction of transistor-to-transistor variations in mobility enhancement. It would be desirable to improve this resolution, possibly using solid or liquid immersion techniques. Micro-XRD is also applied to measure the stress in small structures, but currently the analysis spot is in the 5–10 micron range, making device analysis not yet feasible. Analysis of ellipsometry data for strained Si channels is complicated, since the dielectric function of Si depends on the stress. This relationship (described by the piezo-optical or elasto-optical tensors) is qualitatively understood, but sufficiently accurate quantitative data for fitting ellipsometry data of strained Si channels is lacking. When only considering the UV portion of the ellipsometry spectra, there is some hope in the capability to determine the gate oxide thickness, at least for sufficiently smooth surfaces. For rougher surfaces, there is an additional source of error, since surface roughness enters the ellipsometry analysis in a similar fashion as the native or gate oxide. For accurate gate oxide metrology, the Si surface roughness should be an order of magnitude less than the gate oxide thickness. This is satisfied for bulk Si starting materials, but may cause concerns for measurements on strained Si channels. Confinement effects in the thin Si channel are not yet an issue in the visible and UV portions of the ellipsometry spectra. In principle, ellipsometry should not only be able to determine the Si channel thickness, but also the Ge content of the SiGe buffer underneath. In practice, however, the Ge content determined from ellipsometry data is much too low, possibly due to ignoring the strain effects on the Si dielectric function. On pseudomorphic Si/SiGe heterostructures, ellipsometry is much more successful.

X-ray reflectivity is an attractive alternative to spectroscopic ellipsometry to determine strained Si channel thickness since the refractive index for X-rays is very close to 1 and does not depend on the stress. For Si channel thicknesses of the order of 10–20 nm, a clear series of interference fringes (sometimes accompanied by an additional large-angle peak of unknown origin) is obtained. However, determining the Si channel thickness using commercial software fitting packages does not always yield the correct value (in comparison to TEM). Possibly, this is related to surface roughness that is more difficult to handle for X-ray reflectivity than for spectroscopic ellipsometry because of the smaller wavelength. Experimental concerns about X-ray instrument reliability and alignment are similar to that described for measurements on high-κ gate dielectrics. High-resolution triple-axis X-ray diffraction has been used successfully (using lab and synchrotron X-ray sources) to determine the vertical Si lattice constant in the channel, another measure for the stress in the structures.

A number of microscopy methods are in the research and development phase. These include the point projection microscope (electron holography) and low-energy electron microscopy. Low-energy electron microscopy has been used to study surface science for several years. The application of this method to materials characterization and possibly to inline metrology needs to be studied. A discussion of these methods is provided in the Microscopy Section of the Metrology Roadmap.

One of the five long-term difficult challenges for metrology is structural and elemental analysis at device dimensions. Fulfilling this need will require developing materials characterization methods that provide maps of elemental or chemical distributions at an atomic scale in three dimensions. 3D Atom Probes and similar methods hold promise of providing atom-by-atom maps for small (50-150 nm diameter) needle shaped samples that may be prepared by FIB lift-out techniques. LEAP technology needs further method and data analysis development, and currently has difficulties in measuring non-conductive and heterogeneously-conductive structures with both conducting and non-conducting features. One challenge will be obtaining near 100% detection of each element during data acquisition. Electron tomography is a growing region of interest and is being pursued by both tilt-series and focal series methods in both STEM and TEM. Aberration corrected TEM currently shows promise in this area as smaller and more intense probes may allow increased resolution and signal to noise required for tomographic analysis.

9. METROLOGY FOR EMERGING RESEARCH MATERIALS AND DEVICES

This section covers the materials and device characterization as well as inline measurement needs for emerging materials and devices. (Refer to the Emerging Research Devices chapter) Considerable progress has been made since the last update to the ITRS. Due to the great interest of the ITRS community in graphene, great advances have proven that the atomic structure can be imaged and electrical properties tested for a variety of new devices. We summarize this below.

The Emerging Research Materials and Devices Roadmap lists the cross-cutting metrology needs as follows:

- Characterization and Imaging of Nano-Scale Structures and Composition
- Metrology Needs for Interfaces and Embedded Nano-Structures
- Characterization of Vacancies and Defects in Nano-Scale Structures
- Wafer Level Mapping of Properties of Nanoscale ERM
- Metrology Needs for Simultaneous Spin and Electrical Measurements
- Metrology Needs for Complex Metal Oxide Systems
- Metrology for Molecular Devices
- Metrology Needs for Macromolecular Materials
- Metrology Needs for Directed Self-Assembly
- Modeling and Analysis of Probe-Sample Interactions
- Metrology Needs for Ultra-Scaled Devices
- Metrology for ERM Environmental Safety and Health

This section of the Metrology Roadmap complements the Cross-cutting Metrology needs described in the ERM roadmap by describing the status and research needs for a number of key measurement methods. This section is divided into sub-sections on 3D Atomic Imaging and Spectroscopy, Other Microscopy Needs including Scanned Probe Microscopies, Optical Properties of nanomaterials, and Electrical Characterization for Emerging Materials and Devices.

9.1. Update on Advances in Graphene Metrology

A great number of researchers are working in the area of graphene materials, device, and metrology development. Metrology has been a key enabler for determination of graphene properties. Devices based on RF transistors and other Beyond CMOS devices are being fabricated using cleanroom processing methods. CVD processing provides a facile route to large area graphene. A number of key properties can be routinely measured including layer number, the presence of voids (possibly missing grains), and carrier mobility. Research efforts have shown the effect of graphene proximity to substrates observing boron nitride substrates increase the carrier mobility in graphene compared to that observed using SiO_2/Si substrates.[6] It is now widely recognized that the properties of single layer graphene (SLG) and few layer graphene (FLG) depend on sample cleanliness, the substrate that the graphene sits on, and the stacking configuration of FLG. The properties of bi-layer graphene depend on the stacking pattern and the rotational orientation of the two layers. One of the key needs for graphene is determining the number of layers across the sample. Low energy electron microscopy, Raman spectroscopy, and optical microscopy (when low spatial resolution is required) have all been used to successfully determine the number of layers. The rotational misorientation of bi-layer graphene can be determined using HR-TEM and STM. Electron-hole puddles in single layer graphene (SLG) have been observed using a single electron microscope and attributed to charge inhomogeneities in the SiO_2 layer below.[7] CVD graphene grain size can routinely be measured using dark field TEM.[8] This work illustrates the importance of the properties of the substrate in the overall device properties.

9.2. Update on Advances in Memristor Metrology

Redox memory devices, such as memristors, provide a number of measurement challenges. For example, the physical mechanisms involved in device operation are not well understood. Operation of the TiO_2 based devices seems to involve formation of conducting nanofilaments within the TiO_2 between metal electrodes. Recently, transmission electron microscopy,[9, 10,] synchrotron based scanning transmission X-Ray microscopy (STXM)[11] with chemical analysis using near edge X-Ray absorption fine structure (NEXAFS), and photoemission electron microscope (PEEM)[12] have observed the formation of a stable “Magneli Ti_4O_7 phase” in the TiO_2 dielectric. This characterization is challenging and far from routine. Filament characterization also illustrates the difficulties involved in understanding new materials.

9.3. Comment on the Impact of Nanoscale Dimensions on Metrology

One of most overlooked challenges in metrology is the need for nanoscale materials properties. The materials properties used to measure process variation not only change at the nanoscale, but are themselves altered by surrounding materials. These changes include optical properties (complex refractive index), carrier mobility, and numerous others. For example, the optical properties of the top layer of SOI are thickness dependent below 10 nm. Furthermore, recent data have shown

the optical properties depend on layers deposited above the top SOI film. This dimensional and materials stack dependence points to the need for developing databases of these properties with entries for critical materials stacks. In some instances, it seems that both carrier and phonon confinement impacts numerous properties including dielectric function (complex refractive index), carrier mobility, and thermal transport.

9.4. 3D Atomic Imaging and Spectroscopy

9.4.1. Aberration Corrected TEM and STEM w/ELS

Aberration corrected lens technology has revolutionized transmission and scanning transmission electron microscopy. Commercially available TEM and STEM systems have demonstrated sub 0.1 nm resolution and electron energy loss spectra have located atoms in an atomic column. Aberration corrected STEM systems are approaching 3D atomic resolution as increased convergence angles reduce the depth of focus. This technology has already been applied to nanotechnology. Recently, single layer graphene has been imaged along with defects in the stacking configuration of multilayer graphene. [13, 14,] Some of the achievements of aberration corrected electron microscopy of nanotechnology include:

- Imaging of single layer graphene, layer corrugation, and defects.
- ELS spectra of a single Sr atom in an atomic column of CaTiO3
- Imaging both K and I atoms of a KI crystal inside a carbon nanotube
- Observation of the movement of atoms in nanodots
- Observation of the relationship between the gold atoms in the nanodot gold catalyst and a silicon nanowire.

Advances in *image and spectral modeling* will enable the full potential of aberration correction and associated advances such as energy filters for the electron source and higher energy resolution/electron energy loss. Multi-slice simulations are already being modified for nano-dimensional materials and other applications. These first simulations indicate that the observation of twinning defects in nanowires requires the use of multiple angles of observation. The impact of nano-dimensions on electron diffraction patterns is also interesting. Microscopy of carbon containing samples has moved beyond carbon nanotubes into single layer graphene. Despite all of the above-mentioned advances, microscopy of soft matter remains exceedingly difficult as bonds are more readily broken in molecular samples. Higher energy resolution for ELS is critical to understanding molecular samples.

9.4.2. 3D Atom Probe

The 3D Atom Probe is an advanced version of a field ionization microscope combined with a mass spectrometer capable of atom-by-atom three dimensional reconstruction of a small needle-shaped sample. The sample may be prepared from a device specific site by chemical or plasma etching, or focused ion beam lift-out techniques similar to those commonly used for TEM sample preparation. In the 3D Atom Probe experiment, a needle-shaped sample is placed in close proximity to an electrode and a strong applied field ionizes atoms from the sample tip, ejecting atoms from the sample, and accelerating them through a position sensitive mass spectrometer. The original position of atoms in the sample is determined from geometric considerations and the atomic mass is determined from time of flight. 3D Atom Probe provides a means of measuring the atomic arrangement of free standing wires allowing a method to characterize doping density in nanowires. Non-metallic samples have had difficulties but progress has been made with the addition of laser pulsing. The 3D Atom Probe brings us closer to the dream of atomic mapping in three dimensions. Current detection efficiency is approximately 60% of the atoms ionized and there has been much progress in developing an understanding of local field effects that affect resultant 3D models.

9.4.3. 3D Tomography

As the geometrical complexity of devices continues to increase, there is a growing need to extend the 3D capabilities of tomography techniques to sub-1nm resolutions. Both electron and x-ray tomography can potentially be extended to sub-nm resolution. As with any tomography technique, such imaging requires multiple images at many different angles. Electron tomography has already demonstrated atomic resolution through the use of aberration corrected STEMs. [15] The potential for sub-nm x-ray tomography with its simplified sample preparation requirements has also shown promise with the advances in x-ray optics using Multilayer Laue Lenses. [16]

9.5. OTHER MICROSCOPY NEEDS INCLUDING SCANNING PROBE MICROSCOPY

Assumption—there is a need for characterizing the structure and local properties of current CMOS devices as they scale down in size, as well as for anticipating the metrology requirements of post CMOS device technologies.

9.5.1. PROBES OF LOCAL PROPERTIES WITH HIGH SPATIAL RESOLUTION: OPPORTUNITIES

Scanning Probe Microscopy (SPM) is a platform upon which a variety of local structure/property tools have been developed with spatial resolution spanning 50 nm to 0.1 nm. Scanning Capacitance Microscopy, Spreading Resistance Microscopy and Conductive Tip Atomic Force Microscopy have been optimized for dopant concentration profile measurement with spatial resolution dependent on dopant concentration. Recent developments in SPM involving frequency dependent signals on the sample and tip, and simultaneous perturbation with more than one frequency and/or probe expand the range and resolution of measurements.

Local Measurements Related to Charge and Transport— it is increasingly important to characterize devices in situ and during operation, particularly as a function of frequency. Scanning Impedance Microscopy and Nano Impedance Spectroscopy span 8 orders of magnitude in frequency to quantify interface and defect properties, including charge trapping. Individual defects in molecular nanowires can be detected with these tools, as well as, local contact potential. Scanning Surface Potential Microscopy (also called Kelvin Force Microscopy) can easily map work function variations at the tens of nm scale and can be exploited to characterize FET and interconnect structures. There is recent evidence that the spatial resolution of this technique can be extended to atomic scales. Surface potential variations on high-k dielectric films can be characterized providing insight on interface properties both before and after metallization with a high energy and spatial resolution. Recent SPM observations of quantum dots demonstrated single electron detection indicated the potential for increased energy resolution in highly specialized environments.

Local Measurements Related to Spin— A scanning probe tool, Magnetic Resonance Force Microscopy, has recently demonstrated the detection of single spins with magnetic probes. Further development will determine limitations on spatial resolution and the potential to study spin polarization and characterize spin based devices. At lower sensitivity, Magnetic Force Microscopy can be used to map current flow through devices. To be generally useful the limits of field detection and development of standardized commercially available magnetic tips are required.

Complex Properties—Future generation devices will likely involve a wider materials set, perhaps including organic and biomolecular constituents, and require additional property measurements. Utilizing high frequencies in various detection configurations yields local dielectric constant, electrostriction, piezo-electric coefficient, switching dynamics, etc. These measurements are critical in the development of capacitor based memory and for hybrid device structures, as well as dielectric characterization.

Multiple Modulation and Combined Probes—The combination of multiple measurements is sometimes necessary to isolate properties and is sometimes useful to maximize information. For example electrostatic interactions that occur during magnetic force measurements can be incapacitating. By measuring surface potential at high frequency, nulling it, and measuring magnetic forces at low frequency, the interactions are separated and quantified. This approach can be applied to produce generalized metrology tools.

9.5.2. PROBES OF LOCAL PROPERTIES WITH HIGH SPATIAL RESOLUTION: CHALLENGES

The challenges are implementing these tools on increasingly miniaturized active devices and complex materials systems in an industrial environment and time scale.

General Accessibility— The time it takes to bring a metrology capability from the lab development to commercialization results in a large gap between capability and accessibility. For some companies the design timeline is on the order of 6 years. This is particularly critical now since device research is encompassing new materials for high-k dielectrics, exploring alternative geometries, and looking toward post CMOS technologies. Other mechanisms of accessibility are necessary to meet roadmap requirements.

Increased resolution— In the era of shrinking electronics, a trend toward higher spatial resolution is desirable. For some SPM tools, fundamental principles will limit ultimate resolution. Other tools are so new that limits have not been examined. Recent results in Scanning Kelvin Probe Microscopy suggest that atomic scale resolution is possible for some of the complex property probes. If so, new physics will emerge and theory will be required to interpret the output. There is a potential to increase the energy resolution of most of the measurements, as demonstrated by inelastic tunneling and single electron detection. The maximum energy resolution will be achieved at low temperature, which is a trade off with throughput and convenience.

Tip and Cantilever Technology—Commercial vendors have developed a large toolbox of specialized SPM cantilevers and tips. Reproducibility is often an issue; in some cases yields of good tips are on the order of 30%. More important is the gap between commercially available cantilevers/tips and those required for tool development. This becomes more difficult as the tips envisioned for tool development involve embedded circuitry and complex tip geometries.

Calibration Standards—The lack of calibration standards for nm sized physical structures is a significant problem. At high spatial resolution and under specialized circumstances, atomic structure can be used. Carbon nanotubes have been suggested as a general alternative and can be used for electrostatic property calibration as well. Standard calibration processes should continue to be developed at the nanometer length scale.

9.6. OPTICAL PROPERTIES OF NANOMATERIALS

The optical properties of nano-scale crystalline materials, especially semiconductors, are modified by quantum confinement and surface states. The fundamental expression of the optical response of a material is its dielectric function. The imaginary part of the dielectric function is directly related to the absorption of light. For both direct and indirect band gap materials, the optical response is characterized by critical points where electrons are excited from the top of a valence band to the conduction band. Certain transitions have a strong excitonic nature. These transitions change as one moves from bulk to thin film to nanowires and then nano-dots.

The symmetry of a bulk sample strongly influences both the band structure and the joint density of states. Quantum confinement in one, two, or three dimensions changes the energy of the critical points and the joint density of states. Thus, the shape of imaginary part of the dielectric function of nano-sized materials is altered by the change in the joint density of states and the appearance of new critical points due to the confinement. One interesting example is the emergence of strong anisotropy in silicon nanowires less than 2.2 nm in diameter and the theoretical prediction of new absorption peaks for light polarizations along the wire axis.[17] The nature of optical transitions with a strong excitonic nature are not well understood, and further theoretical and experimental work is required to understand the role of excitons in nanoscale materials.

9.7. ELECTRICAL CHARACTERIZATION FOR EMERGING MATERIALS AND DEVICES

Many emerging nanoelectronic devices exhibit non-conventional behavior such as negative differential resistance and hysteretic switching.[18, 19, 20] New electrical measurement methodologies and analyses will be required to characterize the behavior of these new emerging materials and devices. Certain traditional parameters, such as mobility, are much more challenging to extract at the nanoscale.[21] It is important to determine what parameters are determining final device performance for a given emerging device technology. In addition, the behavior of some categories of emerging devices is based upon completely different mechanisms than those in traditional CMOS. For example certain devices have intrinsically quantum mechanical behavior, while others do not utilize charge transport to change the computational state, but rely upon other mechanisms such as magnetic flux changes. Salient device parameters and their extraction methods will need to be defined for such new devices that switch by different physical principles than standard MOSFET structures. Methodologies will need to be established for characterizing the stability and reliability of new device structures and circuit architectures.

In addition to advances in electrical test methodologies, viable test structures are critically needed to reliably and reproducibly measure nm-sized interfacial elements (such as individual molecules and nm-sized semiconductor quantum dots) incorporating larger electrodes and leads that can be electrically contacted by probes or wire bonds. Methods to contact sub-lithographic components of emerging nanoelectronic devices are perhaps the greatest challenge for the electrical characterization of emerging materials and devices. Furthermore, parametric test structures need to be developed that interrogate the interface between metal interconnect and the active region of nano-scale devices, especially those fabricated with organic materials. Parameters such as work function, barrier height, and transport processes need to be investigated and defined for devices fabricated with unconventional materials.

10. REFERENCE MATERIALS

Reference materials are physical objects with one or more well established properties typically used to calibrate metrology instruments. Reference materials are a critical part of metrology since they establish a "yard stick" for comparison of data taken by different methods, by similar instruments at different locations (internally or externally), or between the model and experiment. Reference materials are also extremely useful in testing and benchmarking instrumentation.

There are two basic kinds of reference materials:

1) A reference material can be a well-calibrated artifact that gives a reference point for the metrology under test.

2) Another equally important reference material tests how accurately the tool under test measures a key process control parameter. The most relevant reference materials are products that come from the manufacturing process. The measurement tools under test (TuT) are designed to measure a feature of a given product such as linewidth accurately, for example. This product contains subtle, but important, process changes that may affect measurement accuracy. It is the responsibility of the metrologist to understand the important process variations that can be difficult to measure by the TuT and to incorporate them into a meaningful set of test artifacts. These test artifacts must then be accurately measured with an appropriately qualified and documented reference measurement system.

Reference materials of the first kind can be obtained from a variety of sources and come in a variety of forms and grades. These types of standards are important and useful, but they tend to be limited in their usefulness because of a limited likeness to the customers' manufacturing process and the lack of relevant induced process variations. Depending on the source, they may be called Certified Reference Materials (CRM), Consensus Reference Materials, NIST Traceable Reference Materials (NTRM®) or Standard Reference Materials (SRM®).[1] The US National Institute of Standards and Technology (NIST) is one of the internationally accepted national authorities of measurement science in the semiconductor industry. Commercial suppliers can also create and submit calibration artifacts to a rigorous measurement program at NIST for the purpose of developing an NTRM; reference material producers adhering to these requirements are allowed to use the NTRM trademark for the series of artifacts checked by NIST.[2]

Another approach is the measurement certification of reference materials through interlaboratory testing under the supervision of recognized standards developing bodies, such as ASTM International. The National Metrology Institutions (NMI) in different countries develop and maintain standards that might be suitable and should be consulted. There is an effort among many of the leading NMIs, including NIST, to coordinate cross comparisons of their measurements and standards to arrive at a mutual recognition sometime in the near future to avoid duplication of efforts.[3]

There are several technical requirements related to reference materials of the first kind and their measurement certification, as follows:

- Reference materials must have properties that remain stable during use; both spatial and temporal variations in the certified material properties must be much smaller than the desired calibration uncertainty.
- Measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. In some areas of metrology no current method of measurement is adequate for the purpose. When the basic measurement process has not been proven, reference materials cannot be produced.
- The final measurement uncertainty in an industry measurement employing a reference material is a combination of uncertainty in the certified value of the reference material and additional uncertainties associated with comparing the reference material to the unknown. For this reason, the uncertainty in the reference material must be smaller than the desired uncertainty of the final measurement. An industry rule of thumb is that uncertainties in the certified value of the reference material be less than ¼ of the variability of the manufacturing process to be evaluated or controlled by the instrument calibrated using the reference material.
- For applications where accurate measurements are required (such as dopant profiling to provide inputs for modeling), the reference material attribute must be determined with an accuracy (including both bias and variability) better than ¼ of the required final accuracy of the measurement for which it will be used.

Additional training of process engineers in the field of measurement science is essential to avoid misuse of reference materials and misinterpretation of the results obtained with their use.

11. REFERENCE MEASUREMENT SYSTEM

A Reference Measurement System (RMS) is an instrument, or a set of several instruments, that complement each other in their ability to excel in various aspects of dimensional metrology. An RMS is well characterized using the best the science and technology of dimensional metrology can offer: applied physics, sound statistics, related standards, and proper handling of all measurement error contributions based on the best protocols available. Because an RMS has been well

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[1] *NTRM® and SRM® acronyms are registered trademarks of NIST.*

[2] *Use of the NTRM mark on a subsequent series of artifacts, even of the same type, requires additional verification testing by NIST.*

[3] *Refer to The International Bureau of Weights and Measures' website http://www.bipm.org/en/convention/mra/.*

characterized, it is more accurate, perhaps by an order of magnitude, and more precise than any instrument in a production fab. An RMS must be sufficiently stable that other measurement systems can be related to it. An RMS can be used to track measurement discrepancies among the metrology instruments of a fab, and to control the performance and matching of production metrology instruments over time.

Due to the performance and reliability expected from this instrument, the RMS requires a significantly higher degree of care, scrutiny, and testing than other fab instruments. Through its measurements this “golden” instrument can help production and reduce costs. However, this is an instrument that, by the nature of the semiconductor process, must reside within the clean environment of the fab so that wafers measured within this instrument can be allowed back into the process stream. Wafers from any other fab can come for measurements and be returned to serve as in-house references across the company or companies.

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